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Characterization of Silicon Deep Reactive Ion Etching Using the SPTS Rapier

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Characterization of Silicon Deep Reactive Ion Etching Using the SPTS Rapier

Summary/Description

This technical report examines the silicon etch process using the SPTS Rapier Si DRIE system and highlights the difference in etch properties between small (~10 micron) and large (~500 micron) features.

Disciplines

Nanoscience and Nanotechnology

	Technical Report	Document No:
	Silicon Deep Reactive Ion Etch (DRIE) Characterization	Revision: Author: Mohsen Azadi, Meredith Metzler, Gerald Lopez

Goal:

The purpose of this document is to examine the etch properties of the SPTS Rapier Si DRIE system and to find the etch rate of Si for different feature sizes.

Materials:

- MicroChem S1818 Photoresist
- MicroChem MF-319 Developer
- 4 inch Silicon Wafers

Equipment:

- Torrey Pines Scientific hotplate
- Reynoldstech spinner
- SUSS MicroTec MA6 Gen3 Mask Aligner
- Oxford PlasmaLab 100 PECVD
- Oxford 80 Plus
- SPTS Rapier Si DRIE Tool

Units:

- Gas flow rate: standard cubic centimeters per minute (sccm)
- Pressure: milliTorr (mT)
- Temperature: degrees Celsius (C)
- High frequency (RF) power: Watts (W)

Protocol:

Deposit

1. Deposit 2.5um of SiO₂ on a blank wafer using a standard recipe (Such as: *“Plasma Enhanced Chemical Vapor Deposition (PECVD) of Silicon Dioxide (SiO₂)”* on scholarly commons)

Coat

1. Mount wafer and ensure that it is centered.
2. Deposit 7 milliliters of S1818 photoresist in the center of the wafer.
3. Spin on photoresist at 4500 RPM for 60 Seconds.

Soft Bake

1. Bake wafer at 130 °C for 180 seconds.

Expose

1. Use a photomask to expose the wafer at 1000 mJ/cm²

Develop

1. Dispense approximately 150 milliliters of MF-319 developer into a six inch cylindrical container.
2. Fully submerge the exposed wafer.
3. Agitate and develop the wafer for 300 seconds.

Hard bake

1. Hard bake at 115°C for 60s.

Etch

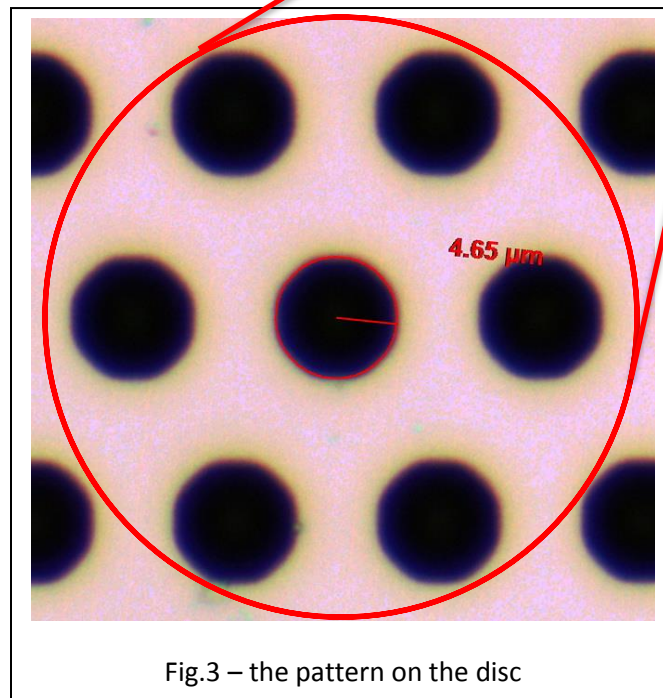
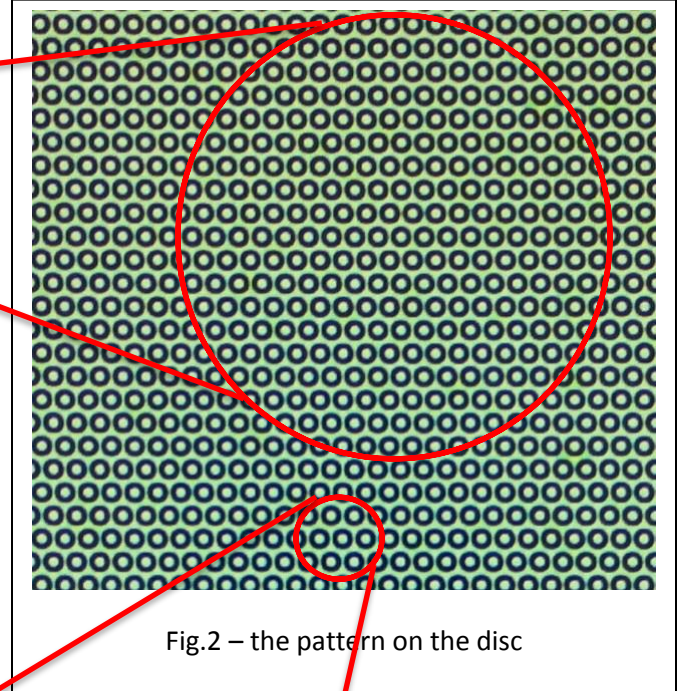
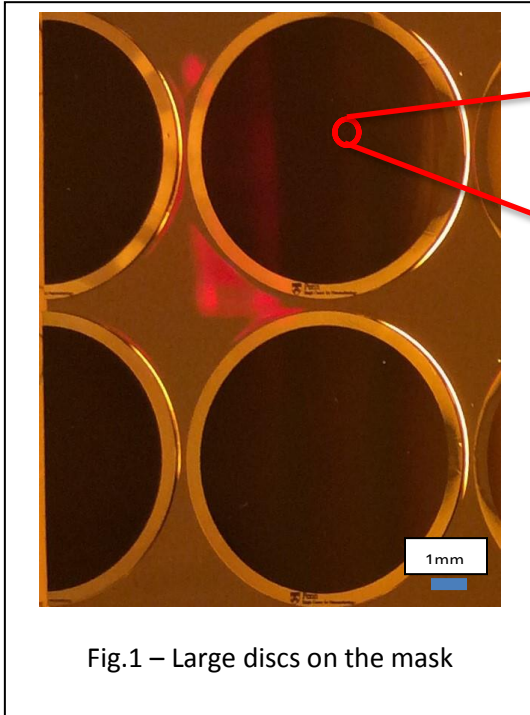
1. Etch through the SiO₂ using the standard procedure such as: “*Reactive Ion Etch (RIE) of Silicon Dioxide (SiO₂) with Trifluoromethane and Oxygen (CHF₃/O₂)*” on Scholarly Commons.

2. Use the following recipe and specify the number of etching loops on the SPTS Rapier Si DRIE tool.

		1	2	3	4
Step Name		Strike 1	Dep 1	Etch 1	Etch 2
Process time	Secs	1.0	1.4 1.4	1.5 1.5 1.5	3.0 3.0
Process Pressure	mTorr	40.0 ± 0%	40.0 40.0 ± 50%	30.0 30.0 ± 50%	30.0 30.0 ± 50%
ACP setpoint position	%	100.0	100.0	100.0	100.0
ACP mode		Automatic	Automatic	Automatic	Automatic
Source power	Watts	2500.0 ± 0%	2500.0 2500.0 ± 50%	2500.0 2500.0 ± 50%	2500.0 2500.0 ± 50%
Source MU tune capacitor		1	4	4	4
Source MU load capacitor		1	1	1	1
Source RF control mode		Load	Load	Load	Load
Source 2 power	Watts	500.0 ± 0%	500.0 500.0 ± 50%	500.0 500.0 ± 50%	500.0 500.0 ± 50%
Source 2 MU tune capacitor		1	1	1	1
Source 2 MU load capacitor		1	1	1	1
Source 2 RF control mode		Load	Load	Load	Load
Platen HF Power	Watts	0.0 ± 0%	0.0 0.0 ± 0%	80.0 80.0 ± 30%	20.0 20.0 ± 40%
Platen HF Capacitor Adjust		Present	Automatic	Automatic	Automatic
Platen HF Tune Capacitor	%	30.0 ± 20%	15.0 ± 5%	15.0 ± 5%	15.0 ± 5%
Platen HF Load Capacitor	%	60.0 ± 20%	35.0 ± 5%	35.0 ± 5%	35.0 ± 5%
Platen HF Padding Capacitor		1	2	2	2
Platen HF control mode		Load	Load	Load	Load
Platen HF modulation Enabled		Enable	Enable	Enable	Enable
Platen HF modulation Frequency	Hz	150	150	150	150
Platen HF modulation duty cycle	%	20	20	20	20
Helium Pressure	Torr	10.0 ± 20%	10.0 10.0 ± 20%	10.0 10.0 ± 20%	10.0 10.0 ± 20%
Helium flow warning level	sccm	8.0	8.0	8.0	8.0
Helium flow fault level	sccm	12.0	12.0	12.0	12.0
Coil current	Amps	10.0 ± 20%	0.0 ± 5%	0.0 ± 5%	0.0 ± 5%
Loop destination		0	0	0	2
Number of loops		0	0	0	*****
Loop variation parameter		0.0	1.0	1.0	1.0
Gas line config		Flow	Flow	Flow	Flow
P1 Ar	sccm	300.0 ± 20%	0.0 0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%
P2 O ₂	sccm	100.0 ± 20%	0.0 0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%
P3 N ₂	sccm	0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%
P4 C ₄ F ₈	sccm	220.0 ± 20%	220.0 220.0 ± 20%	1.0 1.0 ± 0%	1.0 1.0 ± 0%
P5 SF ₆	sccm	1.0 ± 0%	1.0 1.0 ± 0%	400.0 400.0 ± 20%	400.0 400.0 ± 20%
S1	sccm	0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%
S2 C ₄ F ₈	sccm	110.0 ± 20%	110.0 110.0 ± 20%	1.0 1.0 ± 0%	1.0 1.0 ± 0%
S3 SF ₆	sccm	0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%	0.0 0.0 ± 5%

*****: number of etching loops

Figure 1 shows the schematic of the pattern on the mask (a unit cell consisting of 7 circular holes in a honeycomb pattern).



Results for the etching process are shown in the table below:

number of etching loops	Depth of the etch for small features Shown in figure 3 [10 um]	Depth of the etch for large features Space between the discs shown in figure 1 [500um]
0	0	0
20	-----	14.6
40	-----	27.4
80	-----	52.3
150	53	117
250	65	154
300	70	197
375	98	290
450	120	-----

Etching rate for large areas (more than 500um) is shown in figure. 4.

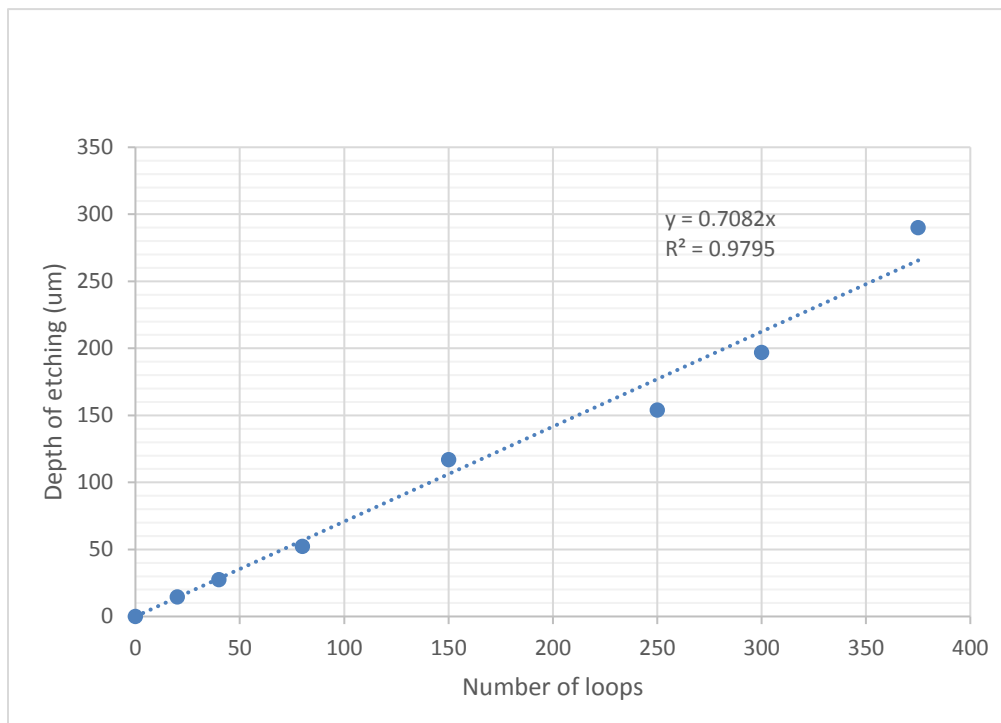


Fig. 4 – etching rate for large areas

Figure 5 shows the rate for large and small areas. (Depth of etching [um] vs the number of etching loops)

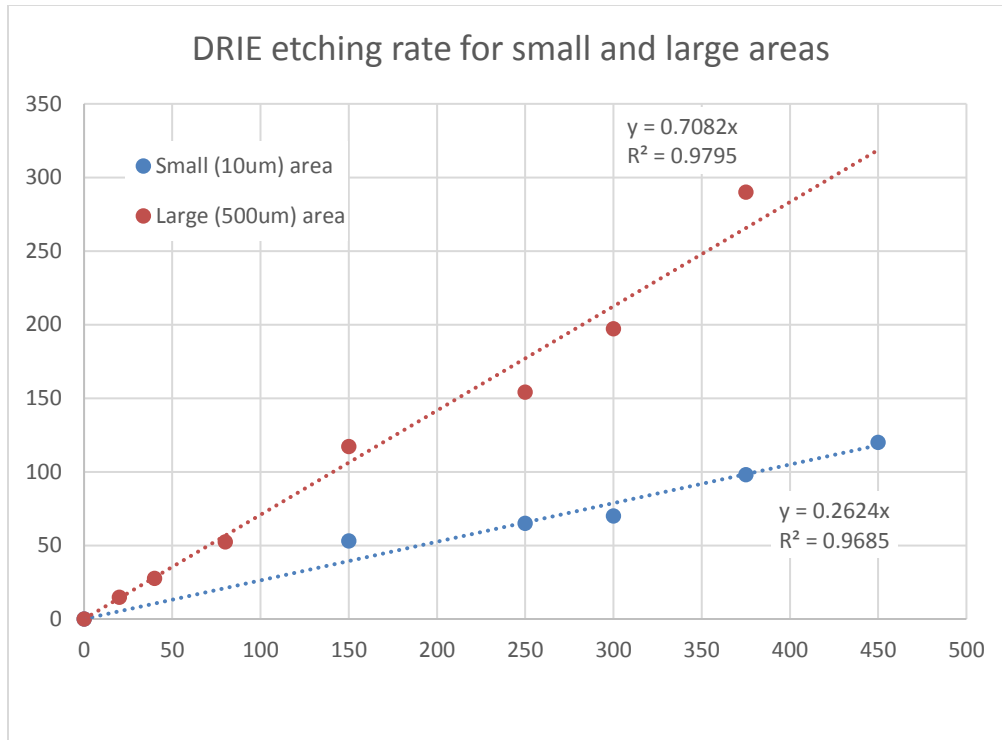
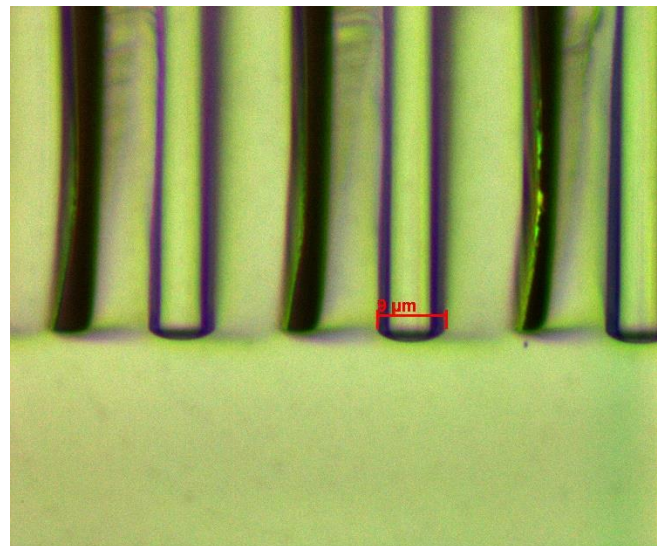
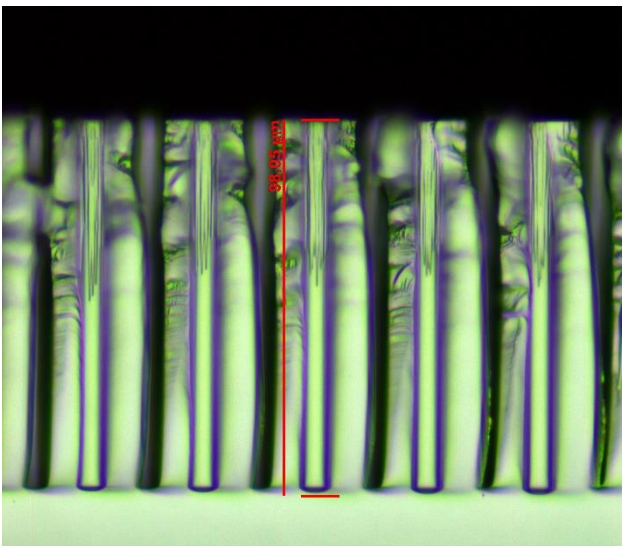


Fig. 5 – Comparison of etch rate of different feature sizes

Figures 6 and 7 show a cross sectional view of the wafer after



Figures 6 and 7 – side views of the patters after 375 loops of etching