Introduction to the Special Section on Nano Systems and Computing

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IT is with great pleasure that we introduce the special section on Nano Systems and Computing to the readership of the *IEEE Transactions on Computers*. This special section consists of five papers that have been selected to cover a wide spectrum of techniques which are encountered in the design of nano-scale computing systems.

We are reaching an interesting time in the physical implementation of computing systems when we can and must contemplate computations built at the molecular and atomic-scale. Continued scaling of our top-down trends suggests features measured in tens of atoms in the next decade, and the discreteness of atomic-scale building blocks is already a present concern in today's advanced ICs. At the same time, scientists are demonstrating new techniques to synthesize designer nanostructures from the bottom up which have small feature sizes and interesting new properties that may expand our device options and our design space.

The physics we need to properly understand and exploit these atomic-scale devices and interconnect structures represents a significant change from the physics which has been adequate for microscale computing systems. These nano-scale systems must consider phenomena such as the statistical behavior of individual electrons, atoms, and molecules, quantum interactions and tunneling, and ballistic transport. Much of the physical phenomena at this scale are known in current science and the challenge is to develop adequate engineering approximations, approaches, and design disciplines to tame them and harness their power; however, many phenomena at this scale are at the edge of or beyond our current scientific understanding.

The result is both new features and capabilities and new concerns and parasitic effects. Opportunities for continuing miniaturization of computing systems are, of course, among the dominant capabilities. Nonetheless, the new devices enabled by nano-scale engineering and different physics also promise new features for new nonlinear devices, nonvolatile state storage, non-charge-based state storage, and superposition of states. Systems built at these scales must accommodate high permanent defect rates, high variation in parameters among devices, high transient fault rates, and continual change in the parameters of individual devices over the operational lifetime of the systems. High variation in parameters reduces our ability for voltage scaling, exacerbating our already significant power-density concerns. For reliable operation, we must manage quantum and thermal parasitics in addition to our growing set of conventional parasitical effects.

It is the convergence of all of the above issues that makes nano-scale computing systems a vibrant and challenging topic for many years ahead. The reader of this special section is provided with a timely account of state-of-the-art research with emphasis on architectures, circuits, and tools.

The first paper of this special section is titled "ZettaRAM: A Power-Scalable DRAM Alternative through Charge-Voltage Decoupling" and is authored by R.K. Venkatesan, A.S. Al-Zawawi, K. Sivasubramanian, and E. Rotenberg. ZettaRAM relies on a new molecular capacitor to provide storage using voltage-independent charge and voltage-dependent speed. In contrast to a traditional DRAM, this enables voltage scaling at low geometries. The architectural features by which this novel type of storage cell can be utilized for L2 cache is analyzed in detail such that, by simple engineering of molecules, voltage scaling and power management are possible through an hybrid write policy.

In the second paper, "Architecture of a Self-Checkpointing Microprocessor that Incorporates Nanomagnetic Devices," L. Kothari and N.P. Carter present a novel architecture of a microprocessor based on magnetoelectronics. This architecture tolerates power failures by periodically checking the state of the currently executing program using on-chip memories. These memories, implemented by magnetoelectronic devices (based on the hybrid Hall effects), are utilized as a (nonvolatile) register file and two buffers for the checking and dirty data. It is shown that this arrangement results in low overhead for power consumption and performance degradation, while attaining high coverage in checkpointing.

The next two papers included in this special section deal with Quantum-dot Cellular Automata (QCA) design and simulation environments. QCA has received considerable attention as it may offer high device density while achieving better power management than other emerging technologies. The first of these two papers is by S. Srivastava and S. Bhanja on "Hierarchical Probabilistic Macromodeling for QCA Circuits." In this paper, a quantitative evaluation of QCA is pursued at the circuit-level. Probabilistic macromodels are proposed using a Bayesian network technique that allows the

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engineer to estimate device level characteristics, such as polarization and low-energy error state configurations. Macromodeling can be used for thermal as well as layout-based analysis. The proposed probabilistic method can be extended to a circuit-level evaluation and is shown to be efficient compared with existing techniques that rely on a full quantum-mechanical simulation of the temporal dynamics.

The next paper, "Neural Network Simulation and Evolutionary Synthesis of QCA Circuits," by O.P. Vilela Neto, M.A.C. Pacheco, and C.R.H. Barbosa, also deals with QCA. In this manuscript, computational intelligence techniques are proposed for simulating QCA circuits; the same techniques can also be used for their synthesis. The utilization of evolvable hardware is proposed and shown to be of great promise for QCA design.

The last paper of this issue is titled "Scaling and Better Approximating Quantum Fourier Transform by Higher Radices," by Z. Zilkic and K. Radecka. This paper considers the realistic scenario by which the Quantum Fourier Transform (QFT) can be utilized with nonbinary quantum circuits. In particular, ternary gates are considered. A new transform is proposed and shown to have better approximation properties than a QFT implemented by binary gates. Error bounds are found and improved in the general case.

We sincerely hope that this special section will be a reference publication for future research. The topics covered in the papers are timely and important, and the authors have done an excellent job of presenting the material. We extend our sincere thanks to all of the authors and reviewers. We also thank Dr. Viktor Prasanna, editor-in-chief of the *IEEE Transactions on Computers*, for allowing us to present this special section. Finally, a special thanks is due to all of the staff for editing and assembling it. Please feel free to contact us if you have questions or comments.

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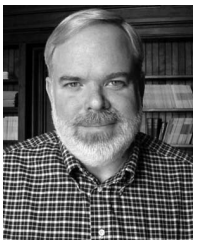
Guest Editors

André DeHon received the SB, SM, and PhD degrees in electrical engineering and computer science from the Massachusetts Institute of Technology in 1990, 1993, and 1996, respectively. From 1996 to 1999, he co-ran the BRASS group in the Computer Science Department at the University of California at Berkeley. From 1999 to 2006, he was an assistant professor of computer science at the California Institute of Technology. Since 2006, he has been an associate professor of electrical and systems engineering at the University of Pennsylvania. He is broadly interested in how we physically implement computations from substrates, including VLSI and molecular electronics, up through architecture, CAD, and programming models. He places special emphasis on spatial programmable architectures (e.g., FPGAs) and interconnect design and optimization. He is a member of the IEEE.



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Fabrizio Lombardi graduated in 1977 from the University of Essex (United Kingdom) with the BSc (Hons.) degree in electronic engineering. In 1977, he joined the Microwave Research Unit at University College London, where he received the master's degree in microwaves and modern optics (1978), the Diploma in microwave engineering (1978), and the PhD degree from the University of London (1982). He is currently the holder of the International Test Conference (ITC) Endowed Chair Professorship at Northeastern University, Boston. At the same institution, during the period 1998-2004, he served as chair of the Department of Electrical and Computer Engineering. Prior to joining Northeastern University, he was a faculty member at Texas Tech University, the University of Colorado-Boulder, and Texas A&M University. Dr. Lombardi has received many professional awards: the Visiting Fellowship at the British Columbia Advanced System Institute, University of Victoria, Canada (1988), the Texas Experimental Engineering Station Research Fellowship twice (1991-1992, 1997-1998) the Halliburton Professorship (1995), the Outstanding Engineering Research Award at Northeastern University (2004), and an International Research Award from the Ministry of Science and Education of Japan (1993-1999). Dr. Lombardi was the recipient of the 1985/86 Research Initiation Award from the IEEE/Engineering Foundation and a Silver Quill Award from Motorola-Austin (1996). Since 2000, he has been an associate editor of *IEEE Design and Test*. He also serves as the chair of the Committee on "Nanotechnology Devices and Systems" of the Test Technology Technical Council of the IEEE (2003-). In the past, he was an associate editor (1996-2000) and the associate editor-in-chief (2000-2006) of the *IEEE Transactions on Computers* and was a Distinguished Visitor of the IEEE-CS twice (1990-1993 and 2001-2004). Since 1 January 2007, he has been the editor-in-chief of the *IEEE Transactions on Computers*. Dr. Lombardi has been involved in organizing many international symposia, conferences, and workshops sponsored by professional organizations as well as a guest editor of special issues in archival journals and magazines such as the *IEEE Transactions on Computers*, *IEEE Transactions on Instrumentation and Measurement*, *IEEE Micro*, and *IEEE Design & Test*. He is the founding general chair of the IEEE Symposium on Network Computing and Applications. His research interests are testing and design of digital systems, bio and nano computing, emerging technologies, defect tolerance, and CAD VLSI. He has extensively published in these areas and coauthored/edited seven books. He is a senior member of the IEEE.