Extremely low drift of resistance and threshold voltage in amorphous phase change nanowire devices

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Time-dependent drift of resistance and threshold voltage in phase change memory (PCM) devices is of concern as it leads to data loss. Electrical drift in amorphous chalcogenides has been argued to be either due to electronic or stress relaxation mechanisms. Here we show that drift in amorphized $Ge_2Sb_2Te_5$ nanowires with exposed surfaces is extremely low in comparison to thin-film devices. However, drift in stressed nanowires embedded under dielectric films is comparable to thin-films. Our results shows that drift in PCM is due to stress relaxation and will help in understanding and controlling drift in PCM devices. © *2010 American Institute of Physics*. [doi:10.1063/1.3447941]

Electric-field induced structural phase transformations in chalcogenides have attracted significant interest due to their potential use in nonvolatile phase change memory (PCM) devices.[1] Chalcogenides (e.g., Ge–Sb–Te alloys) are particularly important for PCM owing to their fast and reversible crystalline to amorphous phase change properties via Joule heating to produce electrically distinct states. However, various challenges including understanding their structural, electronic, thermal, and mechanical properties especially in the amorphous state, the effect of field on electrical switching, and device scalability needs to be addressed before PCM can become a viable alternative to flash technology.

Chalcogenide glasses are affected by relaxation processes that occur on a large distribution of timescales resulting in time-dependent electrical,[2–5] optical,[6] mechanical,[7] and thermal[8] behavior. For PCM device operation, the amorphous state resistance and the field strength at which it switches to a higher conducting state (threshold voltage, V_{th}) are fundamental parameters that determine device reliability. Any phenomenon that affects these critical parameters leading to temporal drift in PCM is an important issue that needs to be investigated[2–4] as they lead to changes in the measurable device characteristics used for recording and reading the information. This issue becomes particularly important for multilevel memory devices, as drifts in resistance would lead to states being overwritten causing serious errors.[9,10] Therefore, it becomes important to understand the physical origin of phenomena that cause drift in material properties to eventually minimize such effects.

The drift of amorphous phase resistance in PCM has been described by a power law,

$$R(t) = R(t_0)(t/t_0)^{\alpha}, \quad (1)$$

where α lies in the range of 0.03 to 0.1 depending on the device type and initial amorphous state resistance.[2–4] However, the drift in V_{th} has been fitted either to a power law,[2,3] or a logarithmic dependence,[4]

$$\frac{\Delta V_{th}(t)}{V_{th}(t_0)} \equiv \frac{V_{th}(t) - V_{th}(t_0)}{V_{th}(t_0)} = \upsilon \ln\frac{t}{t_0}, \quad (2)$$

where υ has been reported in the range of 0.02–0.04.[4]

The fundamental understanding and the origin of amorphous phase drift in PCM are being actively debated and have been explained by a variety of effects including stress relaxation,[2,4] relaxation processes which anneal the electronic defects,[2,3] and the formation of valence alternation pairs (VAP),[11–13] all of which can increase the mobility gap causing an increase in material's resistivity and V_{th}. Within the electronic structural relaxation model, the annealing of traps occurs due to atomic motions that results in an increase in the intertrap distance. The stress relaxation model is based on the built-in internal hydrostatic pressure in the embedded amorphous dome due to the melt-quench process owing to the large difference between the densities of the crystalline and amorphous phase (5%–7%). The slow relaxation of internal stress (volume dilation), consistent with the stress relaxation data,[14] is due to atomic motions within the embedded amorphous dome which increases the Fermi level from the valence band edge causing time-dependent increase in resistance and V_{th}.

One way to distinguish between these proposed mechanisms is to design experiments on unembedded nanoscale systems in which the stress upon amorphization can relax efficiently. The stress relaxation efficiency can also be engineered by changing the surface-to-volume ratio or by embedding the nanodevice without altering the material's electronic properties. If the stress relaxation mechanism dominates the drift dynamics, then any change in the system's ability for efficient stress relaxation should significantly influence its drift characteristics.

Phase change nanowires (NWs) are important materials as they can be reliably connected into devices, their sizes can be controlled down to 10 nm to tune the surface-to-volume ratio, and unlike thin films, NW devices can be configured with their surfaces exposed or completely embedded. Experiments on phase change NWs have shown efficient electrical switching due to material confinement, scalability,[15] multibit operation,[16] and evidence of strong heterogeneous nucleation from its surfaces.[17] Here, we utilize the unique geometry of NWs to understand the mechanism of resistance and V_{th} drift in PCM. It is shown that NW devices have extremely small values of drift coefficients in comparison to thin films. By systematically varying the stress relaxation parameters such as the surface-to-volume ratio of the NWs and comparing unembedded and embedded devices, it is demonstrated that

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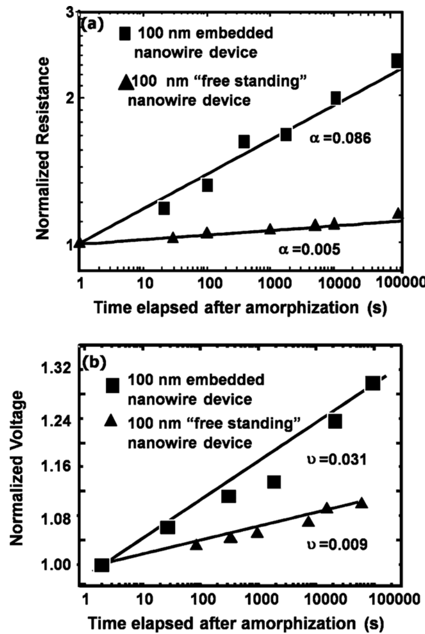

FIG. 1. (a) Time-dependent normalized resistance drift behavior of a 100 nm thick unembedded $Ge_2Sb_2Te_5$ NW device (triangles), and the same device embedded under a 300 nm thick SiO_2 film (squares), amorphized to a resistance of 2.1 MΩ. The solid lines are fit to Eq. (1) and the corresponding drift coefficients are given. (b) Drift of normalized V_{th} for an unembedded (triangles) and the embedded NW device (squares). Solid lines are fit to Eq. (2). The embedded device shows higher drift coefficients in comparison to unembedded devices.

the release of built-in stress upon amorphization is primarily responsible for drift in PCM.

Phase change $Ge_2Sb_2Te_5$ NWs were synthesized using the bottom-up approach of catalyst mediated vapor–liquid–solid process.[15] NW devices were fabricated with Pt electrodes[15] and their resistances were measured at 0.2V (dc). The NW devices were amorphized by 200 ns electrical pulses to resistance values of 1–4 MΩ, and then were allowed to relax over five decades of time during which the resistance was measured at different intervals. For V_{th} drift measurements, dc *I-V* sweeps were measured beyond the V_{th} and the devices were amorphized back to the original resistance for time-dependent measurements.

The time evolution of amorphous state resistance (normalized at t=1 s, first measurement) of a 100 nm thick NW device from the initial value of 2.1 MΩ [Fig. 1(a)] clearly shows that the resistance drift is very small with the resistance increasing to just 2.3 MΩ over five decades in time. The data are fit to a power law [Eq. (1)] with the power exponent, α of 0.005, which is very small in comparison to thin-film devices where α typically ranges from 0.03–0.1.[4] The corresponding data for drift in V_{th} (normalized at 2 s, first measurement) can be fit to Eq. (2) [Fig. 1(b)], which also reveals a lower drift exponent (υ=0.009) in comparison to typical values ranging from 0.01–0.04 in thin films.[4] These experiments demonstrate that drift coefficients are lower in NW devices in comparison to thin-films.

In order to study the correlation of drift coefficients with NW size, we measured the resistance drift on three different NW thicknesses, 140, 90, and 45 nm, all amorphized to resistance values that were ~100 times more than their crystalline state resistance. The NW devices show a systematic size-dependent drift of amorphous state resistance (Fig. 2); the drift coefficients increase with increasing NW thickness.

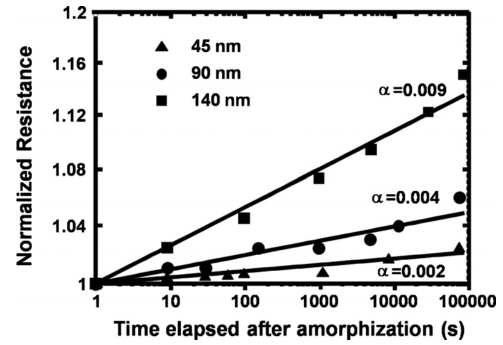

FIG. 2. Size-dependent drift of normalized resistance for $Ge_2Sb_2Te_5$ NW devices. Smaller diameter devices show less drift compared to larger diameter devices. Solid lines are fit to Eq. (1).

The thinnest NW (45 nm) with the highest surface-to-volume ratio shows the lowest drift (α=0.002), while the thickest NW device (140 nm) with the lowest surface-to-volume ratio shows higher drift coefficient (α=0.009) but much smaller than thin-film devices The V_{th} drift coefficients did not reveal any clear size-dependence, mostly because the V_{th} changes typically from ~1.5 V (t=2 s) to ~1.7 V (t=10^5 s) for NW devices, a small increase to reliably extract their size-dependence.

The above described data suggests that the unique geometry of NW devices with exposed surfaces may be responsible for the observed low but size-dependent drift coefficients. In order to explore the effect of exposed surfaces on drift in NWs, we performed measurements on the same NW devices by depositing thick (~300 nm) dielectric films such as SiO_2 or Si_3N_4 on them. The devices were imaged with scanning electron microscopy (SEM) to ensure that they were completely embedded. The same 100 nm NW device as discussed in Fig. 1 but embedded under SiO_2 film was amorphized again to a resistance value of 2.1 MΩ and its resistance drift was measured. The NW device now showed a much higher resistance (α=0.086, compared to 0.005 for unembedded), and V_{th} drift coefficients (υ=0.031, compared to 0.009 for unembedded), which are similar to values reported for embedded thin-film PCM devices (Fig. 1). Similar values of increase in drift coefficients for NWs embedded under Si_3N_4 film in comparison to unembedded devices were obtained (data not shown). These data suggest that the drift characteristics of the devices can be engineered by altering their surface-to-volume ratio and exposing/embedding the surfaces.

Our measurements on NW devices clearly demonstrate the difference in drift behavior as a function of surface-to-volume ratio and exposed surfaces. These observations suggest that the efficient relaxation of the built-in stress upon amorphization is primarily responsible for drift in PCM devices in comparison to annealing of electronic defects or VAP generation mechanisms. In a conventional thin-film PCM device, a polycrystalline film is sandwiched between two electrodes; upon amorphization, a completely embedded amorphous dome results, which is compressed under large stresses from the surrounding materials. In the course of time, the metastable amorphous region relaxes with a large distribution of timescales, which has been mapped with stress relaxation experiments,[14] resulting in a time-dependent increase in resistance and V_{th} due to volume dilation. These relaxations have been extensively studied in glasses and have

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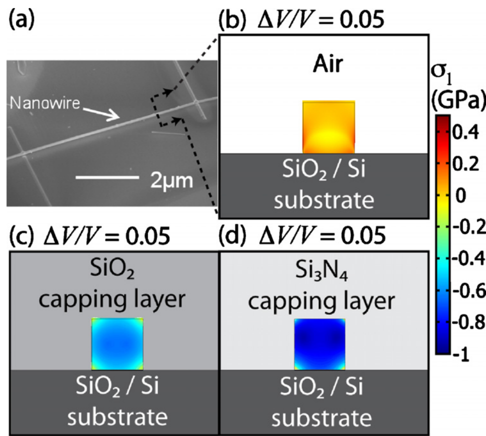

FIG. 3. (Color online) (a) SEM image of an unembedded NW device. [(b)–(d)] Finite element analysis of the elastic first principal stresses that develop in a $Ge_2Sb_2Te_5$ NW cross-section (100×100 nm^2) upon amorphization. A volume change of $\Delta V/V=tr(\varepsilon_{ij})=0.05$ (ε_{ij}, strain tensor), representing the decrease in density upon amorphization, Young's modulus of 35 GPa and Poisson's ratio of 0.3 were used for $Ge_2Sb_2Te_5$ (Ref. 22). An unembedded NW (b) develops small stresses due to adhesion at the substrate interface but large compressive stresses develop in devices confined with SiO_2 (c) and Si_3N_4 (d). These stresses are likely accommodated by relaxation mechanisms in the amorphous material, which influences the drift behavior (Ref. 14). Note that stresses in the substrate and capping layers are present but have been omitted for clarity.

been attributed to atomic relaxations, where unsaturated and distorted bonds in the metastable state relax to more stable states leading to time-dependent mechanical and electrical properties.

Unlike thin-film devices, NW devices do not have a completely embedded amorphized dome, which will enable them to relax their stress rapidly from the large available surface (Fig. 3), leading to very different drift behavior as observed. Typically, phase change NWs have a ~1–2 nm coaxial surface oxide shell which can easily expand when the NW device is locally amorphized thereby releasing the stress. Smaller diameter NWs have large surface-to-volume ratio and can relax their stress more easily. It is known that NWs can be epitaxially grown on highly mismatched substrates and their heterostructures can be created to withstand large strains due to the free surfaces allowing for lateral strain relaxation.[18,19] Theoretical studies on nanostructures have also revealed that strain-relaxation become more efficient with increasing surface-to-volume ratio.[20] For NWs buried under dielectric-films, the situation becomes similar to convention thin-film PCM devices and the amorphous region cannot relax the built-in pressure and hence relaxes slowly on multiple timescales leading to higher drift. This is in agreement with crystallization-induced stress measurements in $Ge_2Sb_2Te_5$ thin-films where the stress was reported to be much higher for capped films.[21] It is unlikely that the deposition of the dielectric-film significantly alters the electronic properties of the NWs as the presence of the thin coaxial oxide layer minimizes their direct interaction. In addition, the drift properties of the embedded NW devices do not appear to be dependent on the dielectric composition, although the drift dependence on the film thickness and stiffness would require further investigation.

We have estimated the elastic stresses associated with the amorphization of the NW geometry for both the embedded and unembedded devices using finite element analysis to provide insight on the relationship between drift and structural confinement. Plane strain two-dimensional calculations were performed on a $Ge_2Sb_2Te_5$ NW cross-section (100×100 nm^2) on a SiO_2 substrate, where the bottom surface of the NW was constrained while the other surfaces were modeled as free [Fig. 3(b)]. The first principal stress σ_1 for the unembedded NW [Fig. 3(b)], reveals that a very small but finite stress develops due to the constraint from the substrate. In contrast, large compressive stresses develop when SiO_2 and Si_3N_4 capping layers are applied [Figs. 3(c) and 3(d)] due to confinement effects upon amorphization, which are ~20 times more than the unembedded case. The low and size-dependent drift coefficients are consistent with the notion of the high surface-to-volume ratio of the NW serving to effectively accommodate the stresses, although a detailed understanding of the atomic relaxation mechanisms in $Ge_2Sb_2Te_5$ NWs requires future investigation.

In conclusion, we have shown that stress relaxation mechanisms are primarily responsible for the observed drift behavior in PCM devices by using unembedded NWs as a model system. The NWs have extremely low values of drift coefficients due to efficient stress relaxation from the exposed free surfaces in comparison to thin-film devices. These results help understand the effect of mechanical stresses on electrical properties of phase change materials and will be useful for the development of improved device geometries that can minimize drift for multilevel memory applications.

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