FULLY INTEGRATED CMOS PHASE-LOCKED LOOP WITH 30MHZ TO 2GHZ LOCKING RANGE AND ±35PS JITTER

Chao Xu, Winslow Sargeant, Kenneth Laker, Jan Van der Spiegel

Department of Electrical Engineering, University of Pennsylvania
200 S 33rd Street, Philadelphia, PA 19104, USA
Email: chaoxu@seas.upenn.edu

Abstract A fully integrated phase-locked loop (PLL) fabricated in a 0.24μm, 2.5v digital CMOS technology is described. The PLL is intended for use in multi-gigabit-per-second clock recovery circuits in fiber-optic communication chip. This PLL first time achieved a very large locking range measured to be from 30MHz up to 2GHz in 0.24um CMOS technology. Also it has very low peak-to-peak jitter less than ±35ps at 1.25GHz output frequency.

1. INTRODUCTION

In recent years, there has been a significant research effort in the area of high-speed electronics for communication. High speeds are required in order to take full advantage of the extremely broadband capabilities of optical fibers. At the same time, the old communication protocols that use different low speeds are still being widely used. In order to lower the cost and to be flexible for the different protocols, a large locking range PLL clock generator is highly needed. In particular, fully integrated CMOS solutions are sought for practical systems to reduce cost and improve reliability. Although a lot of different speed PLLs have been reported recently [1][2][3][4][8], the large locking range from 30 MHz to 2GHz CMOS PLL has not been seen in 0.24um CMOS technology. Also, in many applications, the generated clock signals are used to drive sampling circuits in which the random variation of the sampling instant, or jitter is a critical performance parameter. The low noise jitter PLL is becoming more and more important.

In this paper, a fully integrated PLL, with a large locking range from 30 MHz to 2 GHz, peak–to-peak jitter noise ±35ps at 1.25GHz output frequency is described. In section 2, a newly invented dual-looped architecture is described. In section 3, the design of the voltage control oscillator (VCO) with large tuning range and low jitter noise is presented. The other circuits that make up the completed PLL, such as PFD and charge pump are described in section 4. Finally, measurements and experimental results of the chip are given in section 5 and 6.

2. DUAL–LOOPED PLL ARCHITECTURE

A block diagram of the classical single-looped PLL is shown in figure 1(a). In order to increase the locking range and reduce the output clock jitter, a newly invented dual-looped architecture is used in our design. The block diagram of this new invented architecture is depicted in figure 1(b).

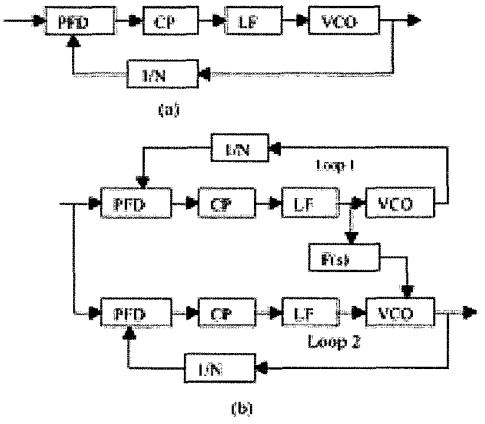

Figure1 (a) Classical single-looped PLL
(b) New dual-looped PLL architecture

The new dual-looped PLL architecture consists of two classical single-looped PLLs, loop1 and loop2. Loop1 is identical to the classical single-looped architecture, as noted in Garden's work [5]. Loop2 is however different by having an extra added control from Loop1. The control signals of the VCO in the loop2 are taken from

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both the output of the loop filter in its own loop (loop2) and from the output of the loop filter in loop1 filtered by F(s). The output system clock is generated from loop2. This newly invented architecture has dramatically increases the PLL locking range and reduces the output clock jitter.

2.1 Improving locking range

In the single-looped PLL, the locking range is limited by the tuning range of the VCO. A very large tuning range VCO is difficult to design because of the need to have it oscillate over the corresponding range. Besides, the stability of the loop phase margin must be maintained. The new dual-looped PLL architecture increases the locking range of the loop2 by having the loop1 provide the DC control voltage to the VCO in the second loop to bring its running frequency close to the locked frequency. The loop2 itself will only need to finely tune the VCO to get the output clock to the desired frequency. From the figure 1(b), one of the control voltages of VCO in loop2 is from the output of loop filter of loop1 filtered by F(s). The purpose of this control voltage is to roughly set the DC control voltage of the VCO2 in order to let the frequency of VCO2 run closely to the locked frequency. It minimizes the phase error in the loop 2 and let the loop2 be able to lock the designed frequency. The new architecture dramatically increases the overall PLL locking range.

2.2 Reducing jitter noise

Jitter noise is another critical performance factor in the design of a high frequency PLL. In the single loop PLL, there is always a tradeoff between large locking range and low jitter noise. In a single loop, the large tuning range of VCO means the large VCO gain $K_{vco}=d\omega/dv$ which means more jitter and phase noise. The newly invented dual-looped architecture uses two loops to solve this design conflict between locking range and the jitter noise. The VCO in loop1 is designed to have a large gain Kvco in order to have a large locking range for loop1. But Loop1 will only provide the DC bias control voltage for loop2. The output system clock is from loop2. So the large VCO gain, i.e. large jitter noise, in loop1 doesn't affect the whole system performance. The VCO in loop2 is designed to have small gain Kvco. Because the loop1 already set the VCO in loop2 to run close to the locked frequency, the loop2 only need to finely tune the VCO frequency around the locked frequency. So it is not necessary for loop2 to have the large VCO gain. Therefore, the new architecture reduces the jitter of the output clock by reducing the VCO gain in the loop2.

Also by having two loops architecture, we can select different loop bandwidths for loop1 and loop2. This affects timing dynamics that might be tailored for each system. The loop having large loop bandwidth will suppress more noise from VCO but it will allow more reference noise to go through. On the other hand a smaller loop bandwidth will suppress more reference noise but let more VCO noise pass through. Two loops give us the design flexibility to select the loop bandwidth of each loop so that we can achieve the optimum desired jitter performance.

3. LARGE RANGE VCO DESIGN

The VCO is designed as a fully differential mode to reduce sensitivity to power supply and substrate noise. The VCO circuit is based on the CMOS ring oscillator that consists of the bias circuit, the differential delay cells and a differential to single ended buffer circuit. The delay cell diagram is shown in figure 2.

The delay cell is based on a N-MOSFET source-coupled pair with voltage-controlled resistor (VCR) load elements that are implemented by the P-MOSFET devices biased in the triode range. The oscillator control current is mirrored into the current sources in such a way that the output-voltage swing across the load remains constant over a wide range of control currents and output frequencies.

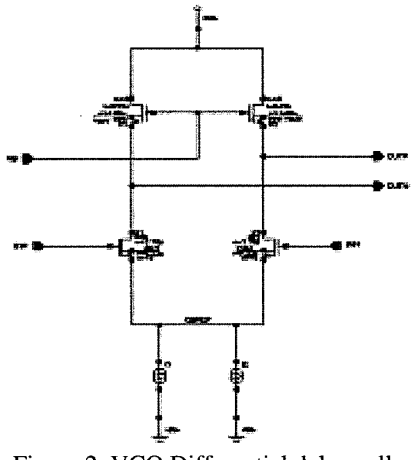

Figure 2. VCO Differential delay cell

In loop2, each delay cell has 2 control current sources. One of them is controlled by the DC

signal from the loop1. This DC control voltage sets the output frequency of the loop 2 close to the locked frequency. And the other control current source is used to finely tune the output frequency to the locked frequency by the loop2 itself.

For N-stage ring oscillator, the gain for each delay cell must satisfy the following condition in order to oscillate.

$$A_v = g_m R \geq \sqrt{1+\tan^2\frac{\pi}{N}}$$

In the design of the bias circuit, a large tuning range requires that the load impedance be adjusted inversely proportional to the g_m. The load impedance R will be changed while we adjust the tail currents by the biased circuit. The goal is to make the A_v almost constant in the whole tuning range. Also the replica bias circuit is used to get the constant swing. The bias circuit is depicted in figure 3.

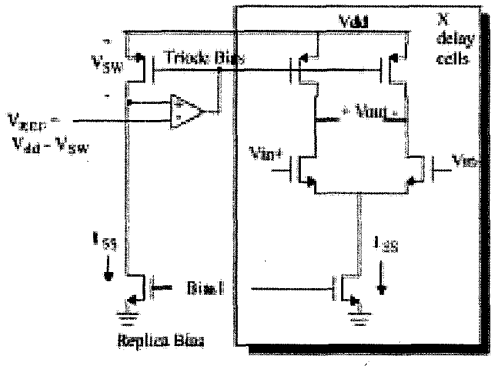

Figure 3. Simplified replica biasing circuit

4. OTHER PLL CIRCUITS

The Phase-Frequency Detector (PFD) used is shown in figure 4. The "dead zone" problem is avoided by adding delays in the loop. The PFD generates two minimum length UP and DOWN pulses, even when the compared waveforms are perfectly synchronized. Those pulses are identical in length, so the up and down currents cancel each other. When the input reference and the feedback clock are not perfectly synchronized, PFD will generate unequal UP and DOWN pulse and let the charge pump to charge the loop filter to adjust the feedback clock phase or frequency.

The charge-pump used is shown in figure 5 [9]. Since the PFD eliminates the "dead zone" by turning both sources on at the same time, a current mismatch between the sources can inject extra noise to the output control node. To avoid variations of the output current due to the output voltage, high-impedance cascode current sources are used.

When the pulse controlling a source is low, normally the source would be turned off. This may cause charge injection at the switching time and slow response. To avoid this problem, the currents are redirected to the output of a unity gain buffer kept at the same voltage as the output of the loop filter. This prevents the current fluctuations that are due to the finite output impedance of the current sources.

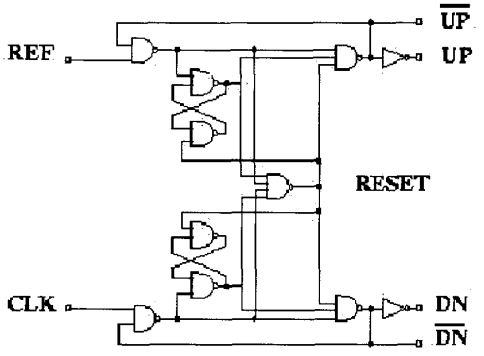

Figure 4: PFD block diagram

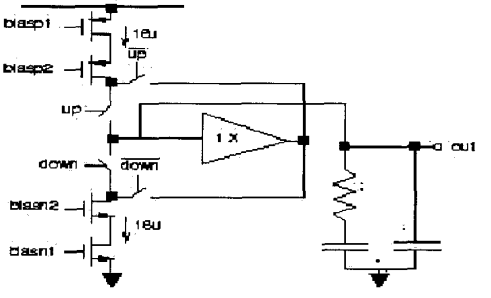

Figure 5. Charge pump circuit

5. MEASURED RESULTS

The following table shows the measured performance of the PLL when functioning with the output frequency running at 1.25GHz.

Peak-to peak jitter	±35ps
Acquisition time	<15μs
Phase margin:	>70°
Power dissipation:	<300mw
Die area:	350x800 μm^2

Figure 6 shows the digital oscilloscope display of the eye diagram of the output clock at 1.25GHz superimposed with a histogram of its jitter. The measured VCO range of the PLL is shown in Figure 7. The range, which is as low as 30 MHz and as high as 2 GHz, has been demonstrated. The figure 8 shows the die micrograph of the PLL.

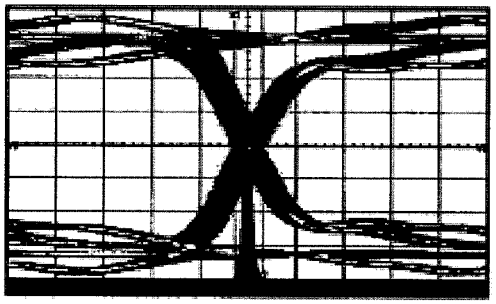

Figure 6 Eye diagram with histogram of jitter

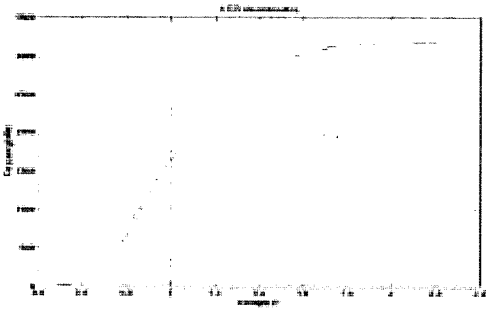

Figure 7. VCO tuning rage

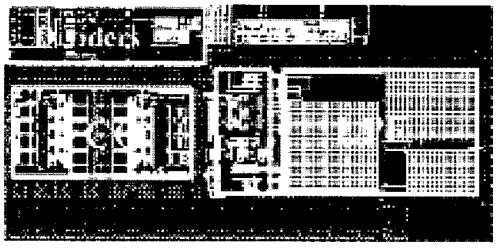

Figure 8. The micrograph of PLL (345x803 μm^2)

6. CONCLUSIONS

A large locking ranges from 30 MHz to 2 GHz PLL has been developed in a digital 0.24um, 2.5V CMOS technology. It is the first time that such a large locking range has been obtained in this technology. The PLL can operate as a part of a noisy logic CMOS chip and is designed to address a wide range of applications. It is fully integrated and has demonstrate lower peak-to-peak of ±35ps jitter at 1.25GHz output frequency.

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