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Disciplines

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Noise Spectral Density Measurements of a Radiation Hardened CMOS Process in the Weak and Moderate Inversion

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Abstract

We have measured the noise of MOS transistors of the United Technology Microelectronics Center (UTMC) 1.2 μm radiation hardened CMOS P-well process from the weak to moderate inversion region. The noise power spectral densities of both NMOS and PMOS devices were measured from 1 KHz to 50 MHz. The bandwidth was chosen such that the important components of the spectral densities such as the white thermal noise and the 1/f noise could be easily resolved and analyzed in detail. The effects of different device terminal DC biases and channel geometries on the noise are described.

I. INTRODUCTION

In general, there has been great interest in understanding the noise characteristics of MOS devices [1] - [10]. For many detector applications, in particular for the readout of silicon strip detectors [8], a low noise and low power input device is required for preamplification. Since the detector (source) impedance is capacitive (of the order 10 - 30 pF), a large ratio of transconductance to total input capacitance, g_m/C_{in}, is required to minimize the device thermal noise. Of equal importance, a large transconductance per unit drain current, g_m/I_D, is required to minimize the device power consumption. With these two constraints, one usually ends up with a device which has a very large width to length ratio, W/L (of the order 1000) and operates in the moderate to weak inversion region. In the literature [1] - [6], most of the noise measurements presented are for devices operating in the strong inversion region. In this paper, we present noise measurement results of MOS devices with varying channel length operating in the weak and moderate inversion regions. The devices were fabricated in a 1.2 μm radiation hardened CMOS process.

II. EQUIVALENT INPUT NOISE SPECTRAL DENSITY

The total drain current noise power spectral density can be written as:

$$\frac{i_d^2}{\Delta f} = 4\,kT\,\gamma\,g_{do} + \frac{B}{f^\alpha} g_m^2 + 4\,kT\,g_{mb}^2\,R_B + 4\,kT\,g_m^2\,R_G \qquad (1)$$

where

γ = the inversion layer thermal noise coefficient
= 2/3 theoretically in saturation for long channel devices in strong inversion [11], [12]
= 1/2 theoretically in saturation for long channel devices in weak inversion

g_{do} = the drain conductance at $V_{DS} = 0$

g_m = the device transconductance

B = the flicker noise coefficient

α = the power of the 1/f noise term (≈ 1)

g_{mb} = the backgate transconductance

R_B = the bulk resistance

R_G = the resistance of the polysilicon gate and the gate interconnects.

The above noise equation is the sum of four components. They are the channel thermal noise, the 1/f noise, the bulk resistance thermal noise, and the gate resistance thermal noise respectively. The value of γ in the transition region (i.e. moderate inversion) between strong and weak inversion regions is expected to vary gradually from 2/3 (strong inversion) to 1/2 (weak inversion). The bulk resistance R_B is a three dimensional distributed resistance located under the channel/inversion layer of the device. The gate resistance R_G is strongly dependent on the gate structure of the device. A brief description of this resistance for our gate structure is presented in section III.

In circuit applications, it is more useful to refer the noise to the input. Assuming a zero source impedance, this can be simply done by dividing the above equation by g_m^2. Thus, the equivalent input noise power spectral density is

$$\frac{v_{in}^2}{\Delta f} = 4\,kT\,\varepsilon\,\frac{1}{g_m} + \frac{B}{f^\alpha} + 4\,kT\,R_B' + 4\,kT\,R_G \qquad (2)$$

where

$$\varepsilon = \gamma \frac{g_{do}}{g_m} \qquad (3.a)$$

$$= \gamma\,(1 + \delta) \qquad (3.b)$$

$1 + \delta$ = the correction term to take into account the effect of fixed bulk charges on g_m [12]

R_B' = the effective bulk noise resistance
$= \frac{g_{mb}^2}{g_m^2} R_B$.

In these noise measurements, we investigate the dependence of ε, B, α, and R_B' on channel lengths, L, channel widths, W, channel areas, WL, drain source voltages, V_{DS}, and reverse

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bias source to bulk voltages, V_{SB}.The conclusions drawn from this study should be applicable to devices from other CMOS processes as well.

It is useful to break the noise expression into two parts: the thermal noise and the 1/f noise. The thermal noise can be rewritten as:

$$\frac{v_{inth}^2}{\Delta f} = 4kT\,R_{eq} \quad (4)$$

where

R_{eq} = equivalent input thermal noise resistance

$$= \varepsilon \frac{1}{g_m} + R_B' + R_G. \quad (5)$$

This equation is the basis for extracting the thermal noise parameters as will be described in section IV.

III. TEST STRUCTURES

Special test devices were fabricated for noise measurement purposes. The test stuctures are a series of transistors of large W/L (up to 1300:1) and varying channel length (1.2 µm - 3.2 µm as drawn). Both NMOS and PMOS devices were fabricated. Their approximate effective channel length, L_{eff} is L_{drawn} - 0.4 µm for NMOS and L_{drawn} - 0.2 µm for PMOS. The gate structure of the transistors is of the interdigitated finger type [10]. A number of transistors of different W and L values were chosen so that:

1. there are several transistors with the same W/L but widely different areas
2. there are transistors of widely varying W/L
3. there are transistors of the same W/L but with L varying from 1.2 µm - 3.2 µm.

The device W/L ratios are: 3996/3.2, 2664/2.2, 1332/1.2, 1332/3.2, 888/2.2, 666/1.7, 444/1.2, 532.8/3.2, 355.2/2.2, and 177.6/1.2. There were 20 devices measured - 10 each for NMOS and PMOS devices.

As mentioned in section II, the gate resistance, R_G of MOS devices is strongly dependent on the actual gate structure. For our interdigitated finger gate structure, R_G is the sum or weighted sum of the resistance of the polysilicon gate, which is distributed in nature, the metal to poly contact resistances, and the gate interconnect polysilicon resistances between one gate strip to another. The expression for R_G can be written as follows:

$$R_G = \frac{N-1}{8N^2} R_I + \frac{N-2}{N^2} R_C + \frac{1}{12N} R_{PG} \quad (6)$$

where

N = the number of gate strips

R_{PG} = the polysilicon gate resistance for each gate strip

$$= (R_{poly}/\text{square}) \frac{W}{LN}$$

R_I = the interconnect resistance between adjacent gate strips = 1.72 . (R_{poly}/square)

R_{poly}/square = 20 Ω/square

R_C = the metal to poly contact resistance = 40 Ω.

As an example, for the largest device we measured, W/L = 3996/3.2 and N = 20, R_G is equal to 7.2 Ω.

IV. MEASUREMENT METHOD AND SET-UP

A. Spectral density measurement

The noise power spectral densities were measured using an HP 4195 A spectrum analyzer. Figure 1 shows the measurement setup. The passive and active electrical components in the measurement system were chosen and biased carefully such that there was enough noise bandwidth (1 KHz to 50 MHz) and the noise current at the drain node (or equivalently the input node of the transimpedance amplifier) of the DUT was dominated by the noise of the DUT. Batteries were used as power supply for the biasing circuits of the DUT.

The drain current noise was fed into a discrete transimpedance amplifier. The resulting noise voltage at the output of the transimpedance amplifier was further amplified

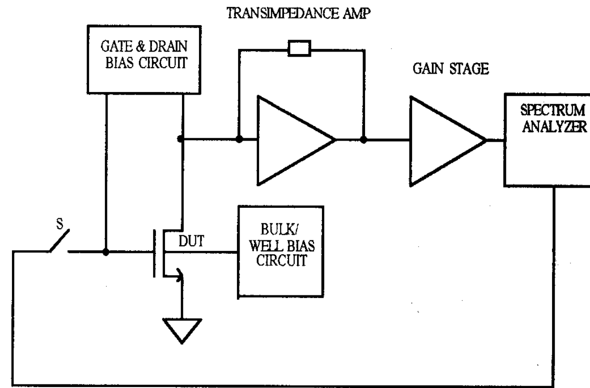

Fig. 1. Block diagram of the spectral density measurement set-up. Noise measurement: The drain current noise of the device under test (DUT) is fed into the transimpedance amplifier (switch S opens). System transfer function measurement: A known signal from the spectrum analyzer is fed into the input of the DUT. (switch S closes).

by a gain stage before it was fed into the input of the spectrum analyzer. If the transimpedance amplifier and the extra gain stage were noiseless, the resulting display on the spectrum analyzer screen would be exactly the drain current noise power spectral density multiplied by a constant gain of the amplifiers following the DUT.

In reality, one has to subtract in quadrature the noise of the rest of the system (i.e. the noise due to the transimpedance amplifier, the biasing circuits, and the gain stage etc.) from the output noise voltage. This extra noise was measured by remeasuring the output noise voltage with the DUT turned off. The output noise voltage spectral density was referred to the input of the DUT (after subtracting the extra noise from it) by dividing it by the overall gain or transfer function of the whole system. The transfer function was measured by feeding a known signal from the spectrum analyzer into the input of the DUT. This input referred noise voltage was the input noise power spectral density of the DUT as described by equation (2). Figure 2 shows a typical spectral

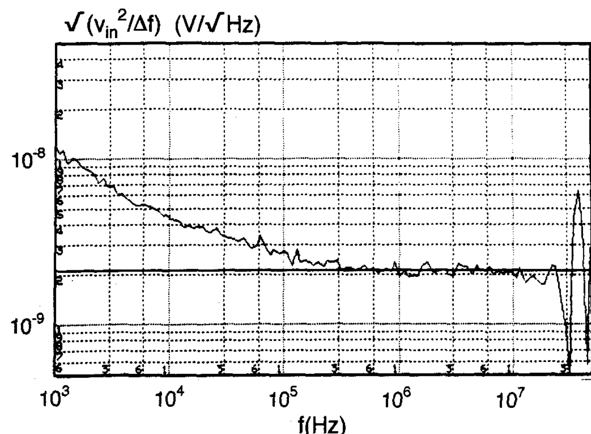

Fig. 2. A typical input noise voltage spectral density. This plot is for NMOS 3996/3.2, $I_D = 300\ \mu A$, $g_m = 4.1$ mA/V, $V_{DS} = 2.0$ V, and $V_{SB} = 0$ V. The spectrum rolls off at about 20 MHz due to the bandwidth of the set-up.

density plot obtained from the spectrum analyzer. From the figure, we extracted the white thermal noise and the 1/f noise.

B. Device electrical parameters measurement

The electrical parameters such as g_m, g_{mb}, threshold voltage and I-V characteristics were measured for each DUT using an HP 4145 B semiconductor parametric analyzer. Only devices with good I-V characteristics were used for the noise measurement.

C. Noise data analysis

As shown in equation (5), the equivalent thermal noise resistance consists of three terms: channel noise resistance, effective bulk resistance, and gate resistance. The gate resistance was modeled accurately as described above. The electrical parameters were measured for each DUT as described above. The terms g_{mb}/g_m and δ for fixed V_{DS} and V_{SB} are approximately constant [12]. Furthermore, these terms are proportional to the bulk doping concentration and inversely proportional to the square root of the reverse bias V_{SB}. Thus, for fixed V_{DS} and V_{SB}, in moderate inversion, the only term that varies in equation (5) is ε.

For each device, the drain bias current was swept and R_{eq} was plotted as a function of $1/g_m$. Theoretically, for long channel devices in moderate inversion (i.e. transistion from strong to weak inversion), the slope ε decreases gradually as $1/g_m$ increases. In our measurements, in the moderate inversion region ($100\ \Omega \leq 1/g_m \leq 300\ \Omega$), the decrease in ε is sufficiently gradual that the measured R_{eq} as a function of $1/g_m$ is still well represented by a straight line. We have therefore fit the data to a linear function to determine the average value of ε in the moderate inversion region. The

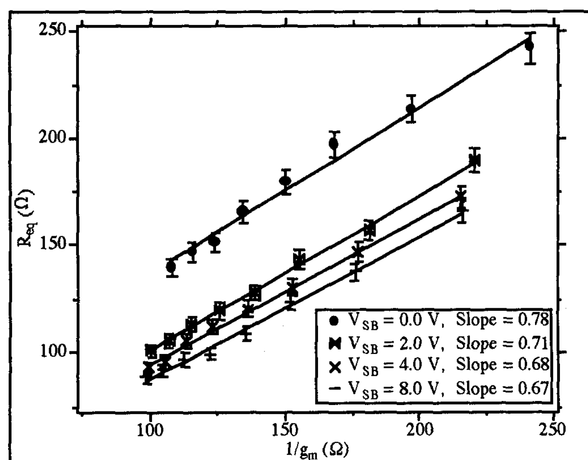

Fig. 3. Equivalent input thermal noise resistance R_{eq} as a function of $1/g_m$ with V_{SB} as a parameter for NMOS 3996/3.2 in moderate inversion (i.e $I_D = 300\ \mu A$ - 1.0 mA). $V_{DS} = 2.0$ V. $R_G = 7.2\ \Omega$. The uncertainty in the slope is about 10 %.

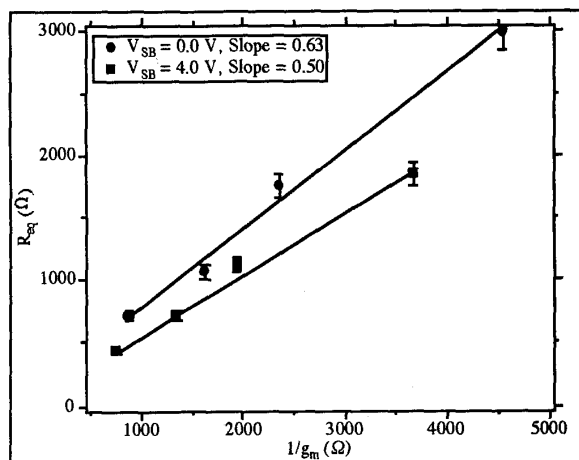

Fig. 4. Equivalent input thermal noise resistance R_{eq} as a function of $1/g_m$ with V_{SB} as a parameter for NMOS 3996/3.2 in weak inversion (i.e $I_D = 10\ \mu A$ - 60 μA). $V_{DS} = 2.0$ V. $R_G = 7.2\ \Omega$. The uncertainty in the slope is about 20 %.

extrapolated y-intercept of this fit line gives an approximate estimate of the noise due to R_G and $R_{B'}$.

V. RESULTS

A. Thermal noise

In this subsection we present a subset of the noise data collected. At the end of this subsection, we summarize the noise parameters extracted from all the data (see Tables I and II). Figure 3 shows the plots of R_{eq} vs. $1/g_m$ for an NMOS device in moderate inversion with W/L of 3996/3.2, $V_{DS} = 2.0$ V, with V_{SB} as a parameter. For each V_{SB}, the slope of the curve is the average value of ε in moderate inversion. The slope decreases as V_{SB} increases because the effect of the fixed bulk charges on g_m decreases [12]. Notice that for a given transconductance, the equivalent input noise resistance drops by about 50 Ω as the reverse bias source to bulk voltage V_{SB}

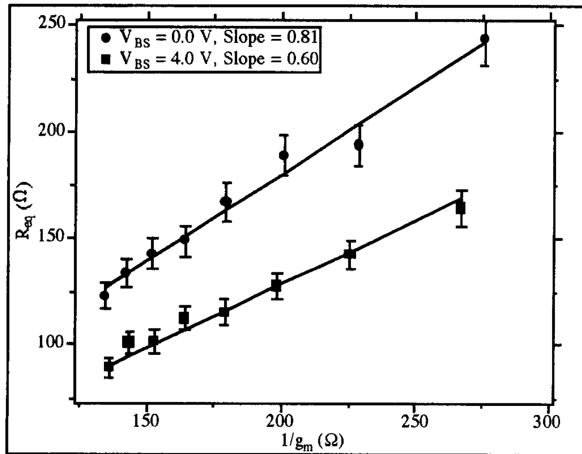

Fig. 5. Equivalent input thermal noise resistance R_{eq} as a function of $1/g_m$ with V_{BS} as a parameter for PMOS 3996/3.2 in moderate inversion (i.e $I_D = 300\ \mu A$ - 1 mA). V_{DS} = - 2.0 V. R_G = 7.2 Ω. The uncertainty in the slope is about 10 %.

is increased from 0 to > 2 V. This is due to a large reduction of the effective noise resistance of the well R_B' through the reduction of $(g_{mb}/g_m)^2$.

Fig. 4 shows the results for the same device in weak inversion. The slope for V_{SB} = 4 V is equal to 0.5 ± 0.1. In this case, the value of ε should be independent of $1/g_m$ because the device operates deep in weak inversion. This value of ε with V_{SB} = 4 V approaches that for bipolar devices (ε for bipolar devices = 0.5) because the effect of fixed bulk charges on g_m is largely reduced.

Figs. 5 and 6 show results for a PMOS device with W/L of 3996/3.2, V_{DS} = - 2.0 V for moderate and weak inversion respectively. The slope for moderate inversion is smaller than that for the NMOS device because the fixed bulk

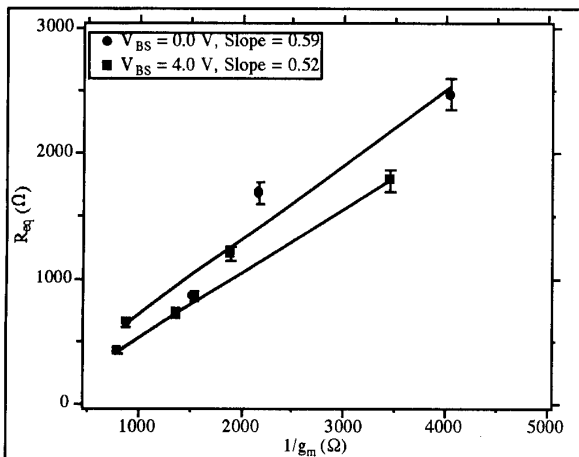

Fig. 6. Equivalent input thermal noise resistance R_{eq} as a function of $1/g_m$ with V_{BS} as a parameter for PMOS 3996/3.2 in weak inversion (i.e $I_D = 10\ \mu A$ - 60 μA). V_{DS} = - 2.0 V. R_G = 7.2 Ω. The uncertainty in the slope is about 20 %.

Table I
Noise parameters for NMOS devices

W/L	Slope†			g_{mb}/g_m ††		
	V_{SB}(V)			V_{SB} (V)		
	0	2	4	0	2	4
3996/3.2 (mod.)	0.78	0.71	0.68	0.61	0.34	0.27
3996/3.2 (weak)	0.63	0.53	0.50	0.61	0.34	0.27
2664/2.2 (mod.)	0.79	0.72	0.64	0.63	0.34	0.26
666/1.7 (mod.)	0.88	0.87	0.85	0.60	0.35	0.26
666/1.7 (weak)	0.77	0.68	0.66	0.60	0.35	0.26
1332/1.2 (mod.)	1.39	1.30	1.00	0.59	0.33	0.25
1332/1.2 (weak)	0.84	0.84	0.82	0.59	0.33	0.25

Table II
Noise parameters for PMOS devices

W/L	Slope †			g_{mb}/g_m††		
	V_{BS}(V)			V_{BS} (V)		
	0	2	4	0	2	4
3996/3.2 (mod)	0.81	0.63	0.60	0.33	0.15	0.11
3996/3.2 (weak)	0.59	0.47	0.52	0.33	0.15	0.11
2664/2.2 (mod)	0.87	0.64	0.66	0.32	0.16	0.12
1332/1.2 (mod)	-	0.99	0.90	-	0.15	0.10

†For moderate inversion, the slope is the average value of ε; the measurement error is ≈ ± 10 %. For weak inversion, the slope is equal to ε; the measurement error is ≈ ± 20 %.
††g_{mb}/g_m was measured directly using HP 4145 B; the measurement error is negligible.

charge effect on g_m is less for PMOS device since the bulk doping for PMOS is smaller than that for NMOS.

It is interesting to compare Fig. 3 to Fig. 5. For a given $1/g_m$ and $|V_{SB}|$, R_{eq} for NMOS is about 25 Ω larger than that for PMOS because $R_{B'}$ is larger for NMOS due to the thinner bulk (well) than that for PMOS (substrate).

Tables I and II summarize the noise parameters extracted from all data. For L ≥ 2.2 μm, the measured slopes within the measurement error agree with the long channel theoretical prediction. The slopes are larger for devices with channel length L ≤ 1.7 μm which suggest that the hot electron effects might have become significant [2], [4]-[6].

B. 1/f noise

The low frequency noise spectral densities of these 20 devices (10 NMOS's and 10 PMOS's) were also measured. The coefficients B and α were extracted for each device. Figs. 7 and 8 show B as a function of $1/(WL_{eff})$ for NMOS and PMOS devices respectively. These figures clearly show that B scales with $1/(WL_{eff})$. From figs. 7 and 8 and the values of C_{ox} for both PMOS and NMOS devices, we calculated the usual parameters K_f for NMOS and PMOS devices as shown in the following 1/f noise expression:

$$\frac{v_{in1/f}^2}{\Delta f} = \frac{K_f}{WL_{eff}\, C_{ox}} \frac{1}{f^{\alpha}} \qquad (7)$$

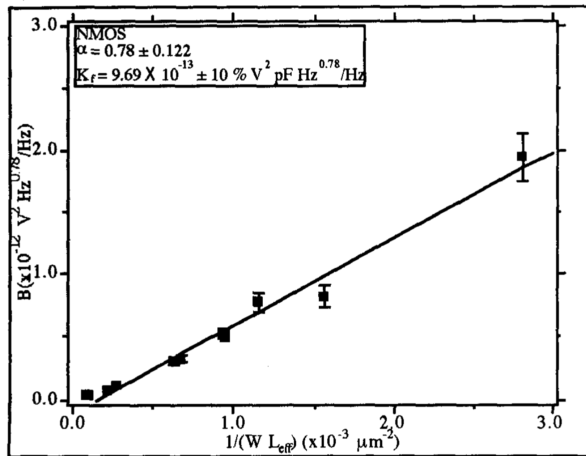

Fig. 7. The flicker noise coefficient B as a function of $1/(WL_{eff})$ for NMOS devices. V_{DS} = 2.0 V, V_{SB} = 4.0 V, C_{ox} = 1.39 fF/μm^2. Bias current density = $I_D/(W/L)$ = 0.8 μA.

The values are $K_f = 9.7 \times 10^{-13} \pm 10\%\ V^2$ pF $Hz^{0.78}$/Hz and $K_f = 8.5 \times 10^{-14} \pm 10\%\ V^2$ pF $Hz^{0.93}$/Hz for NMOS and PMOS devices respectively. A typical value for commercial CMOS process is $3 \times 10^{-12}\ V^2$ pF for NMOS devices [13].

VI. Conclusions

The noise of a radiation hardened 1.2 μm CMOS p-well process was measured in the weak and moderate inversion regions. For $L \geq 2.2$ μm, the channel thermal noise - characterized by the parameter ε - agrees within measurement error with the long channel theoretical prediction. The noise was shown to increase for channel length $L \leq 1.7$ μm due to potentially the hot electron effects in short channel devices. The effective bulk resistance thermal noise was largely reduced with sufficient reverse bias source bulk voltage ($|V_{SB}| \geq 2$ V).

For p-well process, the overall thermal noise for a given $1/g_m$ is better for PMOS devices than that for NMOS devices. This is due to the lower doping concentration of the bulk and the thicker bulk material (substrate) for PMOS devices. In general, it can be concluded that devices which are not in the well would give better thermal noise performance.

The 1/f noise coefficients K_f for this process are very respectable compared to other CMOS processes. For this process, the 1/f noise coefficient K_f for PMOS devices is about 10 times smaller than that for NMOS devices.

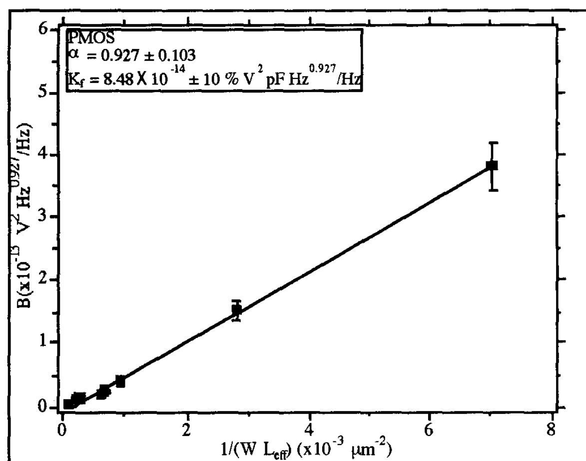

Fig. 8. The flicker noise coefficient B as a function of $1/(WL_{eff})$ for PMOS devices. V_{DS} = - 2.0 V, V_{BS} = 4.0 V, C_{ox} = 1.53fF/μm^2. Bias current density = $I_D/(W/L)$ = 0.8 μA.

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