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A CMOS Time to Digital Converter IC with 2 Level Analog CAM

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Abstract
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Keywords
time to charge converter, CAM, pipelining, associative memory

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A CMOS Time to Digital Converter IC with 2 Level Analog CAM

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Abstract—A time to charge converter IC with an analog memory unit (TCCAMU) has been designed and fabricated in HP's CMOS 1.2-μm n-well process. The TCCAMU is an event driven system designed for front end data acquisition in high energy physics experiments. The chip includes a time to charge converter, analog Level 1 and Level 2 associative memories for input pipelining and data filtering, and an A/D converter. The intervals measured and digitized range from 8-24 ns. Testing of the fabricated chip resulted in an integral nonlinearity of 0.85, a typical differential nonlinearity of < 35 ps, and a typical integral nonlinearity of < 200 ps. The average power dissipation is 8.28 mW per channel. By counting the reference clock, a time resolution of 107 ps over ~ 1 s range could be realized.

I. INTRODUCTION

TIME to digital converters (TDC's) have a variety of industrial and research applications. They are used in time of flight (TOF) measurement systems as well as test equipment for electronic circuit characterization. TOF systems include such examples as laser range finders, positron emission tomographs, and various high energy physics particle detectors. To satisfy the increasingly stringent requirements of data acquisition in colliding beam physics experiments, a VLSI chip called the TCCAMU (time to charge converter with an analog memory unit) has been designed.

In large scale particle detectors, the particle tracks resulting from the beam collisions must be reconstructed as precisely as possible. Straw tube drift chambers, for example, accomplish track reconstruction by measuring electron drift times. The electrons are created when the charged particles being detected ionize the gas in the straw tubes [1]. It is therefore necessary to measure the electron arrival times at each of the drift chamber's many thousands of sense wires. A typical front end readout channel associated with a sense wire is shown in Fig. 1.

The charge signal on a sense wire first must undergo amplification and shaping. If the amount of charge arriving at the wire exceeds a predetermined threshold, a Discriminator (Discr) pulse will be generated. A high resolution TDC must then measure the arrival time of this Discr pulse with respect to an edge of the system clock. The random arrival times of the sense wire signals dictate a TDC double pulse resolution as small as 20-30 ns.

Asynchronous multichannel systems such as this often produce large amounts of data. Since only certain events found by the detectors are of interest, much of the data needs to be discarded at various levels by the front end readout electronics. Data filtering can be accomplished by readout triggers generated external to the front end electronics (Fig. 1). The filtering may occur before and/or after digitization of the signals.

Current generation detectors have ~ 10^5 channels, while future detectors could have even more. Such massive parallelism imposes very strict requirements on the data acquisition circuitry. Typically, the front end readout electronics must have (per channel) a high circuit density, a low power dissipation not more than several tens of mW, TDC resolution < 0.5 ns, TDC double pulse resolution of 20-30 ns, buffers for data filtering, a minimum of calibration constants for each channel, and good gain matching between channels [2].

There are various TDC architectures one might consider using to satisfy these requirements. One type of digital TDC architecture, for instance, uses a feedback stabilized delay line. This type of converter digitizes time intervals very quickly and with a low power dissipation. The LSB width for the Time Memory Cell (TMC) by Arai et al. [3] and similar circuits is typically ~ 1 ns. Feedback stabilized delay lines are more power efficient than high speed counters or shift registers for time measurements.

A second TDC approach involves a digital vernier technique [4]. Short time intervals are expanded by beat signals and then interpolated. Essentially this gives a very high resolution measurement of the delay between 2 periodic signals. While...
the digital vernier TDC can achieve ~ 1 ps resolution using bipolar technology, it would not be practical in systems with an asynchronous single pulse input.

A third approach is based on an analog technique, such as that discussed by Stevens [5]. By integrating a current "I" on a capacitor during the time interval being measured, we have a time to voltage converter. The resulting voltage can then be digitized. Although this technique can be more complicated to implement than the stabilized delay line architecture, it does achieve sub-nanosecond resolution in addition to low power dissipation. This analog approach can be subdivided into two groups: those analog TDC's using a time-to-voltage converter (TVC) and those using a time-to-charge converter (TCC).

The TCC, which is part of a dual slope converter, is well suited for massively parallel data acquisition systems. It has the advantages over the TVC of insensitivity to capacitor and integration current variations, and a calibrationless gain. The TCCAMU chip discussed in Section II utilizes a CMOS TCC, giving it a very low power dissipation and a subnanosecond resolution.

II. TCCAMU ARCHITECTURE

A. Overview of TCCAMU

The TCCAMU measures time intervals, stores and filters the measured data in analog memory, and finally performs a digitization. The interval to be measured occurs between the leading edge of an asynchronous Discr pulse and an edge of the system clock. The system clock frequency for the TCCAMU is 62.5 MHz (16-ns period). By counting the clock cycles, it should be possible to accurately determine the arrival time of a Discr pulse over a wide dynamic range.

A time to charge conversion starts with a Discr pulse activating one of two width generators (Fig. 2). The even and odd generators take turns accepting Discr inputs, resulting in time measurements with improved double pulse resolution. The selected width generator generates an output pulse whose width equals the interval being measured. For the duration of this output pulse, the TCCAMU steers a current "I" onto an integration capacitor in its analog memory. The resulting charge is proportional to the measured time interval.

The analog associative memory which stores and filters the charge data consists of Level 1 and Level 2 buffers. The read/write locations in both buffers are chosen by the Level 1 Read/Write counters and the Level 2 Read/Write counters. The outputs of the counters are decoded by control logic to select the proper capacitors in the associative memory.

The signal from a time to charge conversion is stored initially in Level 1 for 1 μs. Because only a fraction of the events found by a particle detector will be useful, the system external to the chip will usually decide to discard the signal during that 1 μs. Signals that are kept are transferred to Level 2 for a longer term storage. Additional filtering in Level 2 decided by the external system occurs before the actual digitization.

The Level 1 delay generator shown in Fig. 2 determines the storage time in the Level 1 analog buffer. A Discr pulse applied to the L1 delay generator input produces an output pulse 1 μs later. If the external system decides to keep the signal during that time, a Level 1 readout trigger called L1OK (Level 1 datum OK) is given to the chip at the end of that 1 μs delay. This in turn causes the Level 1 datum to be transferred to the Level 2 analog memory. If the L1OK pulse were not present at the end of that 1 μs, the Level 1 signal would be discarded. Future chip versions could contain a programmable L1 delay generator, yielding an adjustable L1 trigger latency for the TCCAMU.

Note the absence of a Level 2 delay generator. The latency in the Level 2 buffer is not predetermined.

Any signal that passes through both levels of the analog memory will then be digitized by the on chip Wilkinson A/D converter. A current "I/150" discharges the appropriate storage capacitor while the number of clock cycles are counted, resulting in an output digital word.

An important issue here is that the analog variable being stored and digitized is a charge, not a voltage. The TCCAMU gain therefore depends on the ratio of the charge and discharge currents, "I" and "I/150" respectively. This ratio can be made relatively process insensitive. Mismatches between channels in the integrating current "I" have little effect on the TDC gain matching. Mismatches in the integrating capacitors within and between channels also have little effect. Gain calibrations for the TCCAMU in a multichannel system would therefore be unnecessary.

For TDC's using a time-to-voltage converter (TVC), on the other hand, it is the capacitor voltage that is digitized. The gain would depend on the absolute value of the integrating current and the integrating capacitors. For multichannel systems, it can be cumbersome dealing with gain mismatches and gain drifts.

B. Width Generator

The time interval Δt to be measured and digitized by the TCCAMU occurs between a Discr pulse's leading edge and a rising edge of the system clock. The width generator (Fig. 3) produces an output pulse of width Δt, leading to a charge Δt being placed on the appropriate storage capacitor.

The capacitors in the analog memory are reset to a reference level prior to the time to charge conversion (reset switches are not shown). During the standing state, transistor M is on and transistors M0 – MN are off. When the width generator
detects a Discr input pulse, it STARTS the integration as the current "I" is steered to the selected capacitor. The width generator waits for a falling clock edge, and then uses the rising clock edge after that to STOP the integration (see Fig. 4(b)). This waiting feature gives us a pulse width range of \( 8 \text{ ns} < \Delta t < 24 \text{ ns} \), thereby avoiding any nonlinearities due to zero integration times.

A simplified schematic for a width generator and the relevant waveforms are shown in Fig. 4. Much of the circuitry in the generator is devoted to determining which rising clock edge will stop the integration. The Discr enters the one shot, which guarantees a minimum pulse width at the source of \( M_1 \). When the clock goes high, node \( A \) also goes high, causing the comparator output \( V_o \) to switch high. When the clock then goes low, node \( B \) goes high. The next rising clock edge then generates the STOP signal, which resets the one-shot.

The important issue of metastability arises here when the falling clock edge occurs at the same time as the rising Discr edge. Transistor \( M_1 \) will start turning off just as the output of the one-shot begins to raise \( M_1 \)'s drain voltage. This case would produce an analog voltage at node \( A \) instead of a well-defined logic level. The width generator could then become metastable, resulting in an arbitrarily wide pulse output. When the \( \text{CLK} \) goes low, however, \( M_2 \) closes the positive feedback loop. This forces the comparator to resolve the analog voltage to a valid logic level usually within 1/2 clock cycle. A positive feedback loop therefore greatly reduces the range of Discr arrival times that cause metastable behavior.

In order to reduce the comparator's area and eliminate its dc power dissipation, the "comparator" was made to consist merely of 2 inverters in series. The feedback switch \( M_2 \) connects the output \( V_o \) of the second inverter to the input \( A \) of the first. The voltage \( V_M \) shown in Fig. 4(a) is actually the metastable voltage for these 2 inverters when \( A = V_o \). When \( M_2 \) closes, the comparator produces a logic "1" if \( V_o > V_M \) and a logic "0" if \( V_o < V_M \).

### C. Analog Input Pipeline with Data Filtering

In asynchronous systems such as particle detectors, the Discr input to a TDC arrives at random points in time. The question naturally arises as to how we can handle the worst case Discr input rates. For this discussion, let:

- \( D T_{\text{MIN}} \) minimum time between successive Discr arrivals,
- \( D T_{\text{AVE}} \) average time between successive Discr arrivals,
- \( C T \) conversion time for a digitization, and
- \( S \) Discr rejection factor.

\( D T_{\text{MIN}} \) is the double pulse resolution requirement of the TDC, which equals 20-30 ns. The average time \( D T_{\text{AVE}} \) between successive Discr arrivals is assumed to be \( \sim 100-200 \text{ ns} \). Only 1 in \( S \) Discr inputs are left over after data filtering in the detector front end electronics, where typically \( S \sim 10^4-10^6 \). The filtering can be accomplished before and/or after the time interval digitization.

Given the average and the maximum input rates to a TDC, we can make one of several choices. Assuming we wanted to digitize all the incoming data, we could use a flash TDC where \( C T < D T_{\text{MIN}} \). This condition would guarantee that data never arrives faster than the converter can handle. The disadvantages of the flash converter, however, are its
complexity, a large power dissipation, and a large chip area. In massively parallel data acquisition systems, a very high speed TDC would not necessarily be the most efficient approach.

An alternative would be to use an analog memory which stores the incoming data before digitization. This is analogous to a pipelined sample and hold in a voltage sampling A/D converter. We would thus have the more relaxed requirement of $CT < DT_{AVE}$. On those occasions when $CT > DT$, the data would simply pile up in the analog buffer until serviced by the A/D converter. The TCCAMU uses this approach.

The speed requirements for an input pipelined TDC are easier to satisfy. This approach requires a much simpler A/D with less power dissipation and less chip area. The reduced complexity of the circuitry would allow a number of TDC channels to be placed on a single die substrate for use in a high density front end readout system.

Additional advantages in using analog input buffers have to do with the data filtering. Obviously, it would be much more power efficient to decimate in an analog pipeline before digitization. Using the rejection factor, we also see that the converter now would need to satisfy the condition $CT < (S) \times DT_{AVE}$ where $S >> 1$.

Note that there will be occasions when the pipeline overflows due its finite size and the finite $CT$. One can determine the minimum number of storage locations needed in the pipeline using queuing theory or Monte Carlo simulations [6]. The minimum size of the analog buffer will be determined by a number of factors: $DT_{MIN}, DT_{AVE}, CT, S$, the storage time in the analog pipeline (or queue), the maximum acceptable probability that the pipeline will be full when a Discr input arrives, and of course the probability distribution for the Discr arrival times.

D. Two Level Analog Content Addressable Memory

The analog memory in the TCCAMU consists of 12 shielded storage capacitors. The capacitors use the gates of PMOS transistors placed in an isolated n-well. These 12 storage devices are part of a 2-level analog content addressable memory (CAM). The CAM is used to implement the analog input pipeline.

In general, an analog CAM has write, read, and match functions. A write operation stores analog information in unused word locations. A match operation involves a parallel search through all the stored words for a match with the input word. The read operation returns the analog information associated with the matched word [7].

In the TCCAMU chip, the analog CAM is divided into 2 levels: Level 1 and Level 2. The Level 1 buffer accesses 8 storage capacitors and the Level 2 buffer accesses 4. A data register is assigned to each of the analog storage capacitors holds a unique address and ID tag. A capacitor, therefore, is chosen for read/write operations according to the contents of its data register. The ID tag contains by register $i$ identifies the level (1 or 2) that capacitor $i$ is associated with, and the address contained by register $i$ is the address within that level.

Because the contents of data register $i$ can be changed, it is possible to "move" the data on capacitor $i$ from one CAM level to another without actually disturbing the analog information on that capacitor. This is the reason for choosing an analog CAM over an analog RAM.

The two-level analog CAM outlined in Fig. 5 has simultaneous Read/Write capabilities for both levels. During the CAM's Level 1 write operation, the charge generated by a time measurement is placed on the capacitor whose Level 1 address matches the address chosen by the Level 1 Write counter (Fig. 2). Let this be referred to as address $j$. After a $\mu s$ latency, a Level 1 Read operation occurs whereby address $j$ for that capacitor now matches the address given by the Level 1 Read counter. An $L_1$ readout trigger will then determine whether to discard the $L_1$ datum being read ($L_1$ reject) or to accept the datum for further processing ($L_1$ accept). An $L_1$ accept results in the data register contents being changed from a Level 1 address $j$ to a Level 2 address $k$. The Level 2 Write counter determines the address $k$ that is loaded into the register. This operation of transferring analog data from address $j$ in Level 1 to address $k$ in Level 2 can simply be called a virtual Level 1 to Level 2 transfer. After an undetermined latency, the Level 2 Read counter will choose address $k$ for a Level 2 read operation. A Level 2 readout trigger can then accept or reject that datum. If it is accepted, the analog data at address $k$ will be digitized. The TCCAMU thus has 2 levels of filtering prior to digitizing a measured time interval.

Note that there are several requirements for a Level 1 to Level 2 transfer. First of all, the transfer must be accomplished quickly so that the Level 1 address $j$ can be made available for writing again. Secondly, we do not want the analog information being transferred to be corrupted by the transfer process itself. Thirdly, we should dissipate as little power as possible to minimize the total power of the multichannel system.

A virtual Level 1 to Level 2 transfer satisfies the previous requirements. Instead of transferring the charge itself from one capacitor to another (as in an analog RAM), we have the data registers for the $L_1$ Read capacitor and the $L_2$ Write capacitor swap their contents. As a result, the analog information on a capacitor is never disturbed during a $L_1$ Read or $L_2$ Write operation. Hence there is no need for any high
power unity gain amplifiers to do a fast charge transfer, since these amplifiers would introduce unwanted gain and offset errors.

E. Control Logic for the Analog Memory

Each capacitor in the analog memory has a control logic circuit (Fig. 6). Each control block can select its capacitor for reading and writing. The logic basically consists of a latch, which contains the storage capacitor's virtual address, and 4 address comparators. The comparators check for a match between the latch contents and the Level 1/Level 2 Read/Write addresses.

The capacitors in the analog memory are accessed for read/write operations according to the contents of their address latches. Hence we have a content addressable memory. Each latch contains a unique address so that no two capacitors undergo the same operation at the same time.

Bits 0–2 of the master–slave latch hold the virtual address, and Bit 3 contains the ID tag. When the capacitor belongs to the Level 1 CAM, the ID tag = 0. The Level 2 CAM has an ID tag = 1.

Comparators #1 and #2 select the capacitor for Level 1 Write and Level 2 Read operations, respectively. In a Level 1 Write operation, the "Write Select" output (even or odd) of the control logic permits the width generator (even or odd) to place charge on that capacitor. In a Level 2 Read operation, the "Read Select" output permits the Wilkinson A/D to remove charge from the capacitor during a digitization.

Comparators #3 and #4 select the capacitor for Level 2 Write and Level 1 Read operations, respectively. They choose the 2 capacitors that will swap virtual addresses during a Level 1 to Level 2 data transfer. For the capacitor whose comparator #3 sees a match between its latch contents and the Level 1 Read address, the multiplexer passes the Level 2 Write address to the latch input. For the other capacitor whose comparator #4 sees a match between its latch contents and the Level 2 Write address, the multiplexer passes the Level 1 Read address to the latch input. When the signal Transfer then goes low, these two latches accept their inputs to complete the Level 1 to Level 2 transfer.

III. Experimental Results

The TCCAMU shown in Fig. 7 has been fabricated in HP's CMOS 1.2-μm n-well process, and has been tested with an HP82000 chip tester. This 2.0 mm x 2.2 mm circuit has 9700 transistors, with 8 storage locations in its analog Level 1 CAM, and 4 storage locations in its analog Level 2 CAM. The digital logic in this IC operates between -3 V and 0 V power supplies, while the analog circuitry operates between -3 V and +3 V.

The average power dissipation during A/D conversions was measured to be 8.28 mW/channel. The L1 delay generator, consisting of numerous clocked shift registers, dissipates ~3 mW according to simulations. The current mirror uses ~0.75 mW, and the on chip A/D dissipates the rest of the power.

Measurements to test the analog memory revealed a charge leakage of 1 LSB roughly every 25 s at room temperature. Signals placed on any given capacitor did not influence the data on any adjacent storage capacitors. Due to the analog input pipeline, the TCCAMU achieved a double pulse resolution between 16–32 ns, despite a 4-μs conversion time.

The differential nonlinearity (DNL) of an A/D converter can be defined as the difference between the actual width of an output code and the ideal width of that code. The DNL of the TCCAMU was measured using a code density test (see Appendix). In this particular test, the probability distribution of the randomized Discr input was a Gaussian. A histogram of the outputs was produced, and the widths and DNL's of the output codes were calculated from this information. Typically the DNL at any given analog storage site was measured to be < 35 ps (see Fig. 8), and the rms DNL over all output codes was 10 ps rms. Using 1000 input samples to measure the width of each LSB, we obtained an uncertainty in the DNL measurements of < 8.5 ps rms.
Note that at the sudden low to high output transition the width generators must decide whether to generate a maximum or a minimum width pulse. A metastable state at this transition exists where the width generators cannot decide which pulse width to create. This state of indecision will occur when a Discr input lands in a very narrow time window centered at that transition. Measurements of the TCCAMU output did not reveal any metastability near this region, however, meaning that the width of the metastable time window must be $<< 1$ LSB. The narrow width of this window results from the use of a positive feedback loop in the width generators. According to SPICE simulations, the width of the metastable window should be $< 10$ ps.

The slope of the output curve in Fig. 9 is $\sim 1$ LSB/107 ps. Because of the independence from capacitor and integrating current mismatches, the channel to channel (i.e., chip-to-chip) variations in the slope are $< 0.2\%$.

The integral nonlinearity (INL) can be defined as the difference between the measured output data and the best fit straight line through that data. The INL was calculated from the curve in Fig. 9. The typical INL for any given analog storage location is $< 200$ ps, with a typical rms INL of 90 ps rms (see Fig. 10). The overall pattern of the INL curve is very similar from capacitor to capacitor, and even chip-to-chip. It is believed that this pattern noise stems from on-chip coupling effects between sensitive signal paths.

The random noise referred back to the input Discr consists of quantization noise and jitter. The quantization noise of the TCCAMU is calculated to be $\sim 31$ ps rms. The jitter of our time to digital converter, due to thermal noise sources, was measured to be $\sim 25$ ps rms. Combining both factors gives a total TCCAMU input referred random noise of 40 ps rms.

The maximum pedestal offset between any 2 analog storage locations in a given chip is $< 8$ LSB’s. The offsets, however, are not due to any mismatches in the capacitors themselves. Rather, the offsets result from a combination of mismatches in the input and output switches of the storage capacitors, and the large parasitic capacitance of the common bus connecting those switches. Efforts are currently underway to reduce these offsets to an expected value of $\sim 1$ LSB.

IV. CONCLUSION

A time to charge converter with an analog memory unit (TCCAMU) and an on-chip A/D converter has been successfully designed, fabricated, and characterized. This IC measures the delay between the leading edge of an asynchronous Discr signal and a following edge of a 62.5 MHz system clock. The analog information from the time to charge conversion is pipelined in a two level analog CAM (content addressable memory). The data in Levels 1 and 2 of the CAM are filtered by externally generated Level 1 and Level 2 readout triggers. After a Level 2 accept, the analog information is digitized. The TCCAMU was fabricated in HP’s 1.2-μm n-well, double metal process. This 2.0 mm x 2.2 mm circuit was verified to be capable of measuring and digitizing its entire 16 ns input range with a $\sim 107$ ps / LSB resolution. Despite its 4-μs conversion time, this chip achieves a double pulse resolution of 16-32 ns by using an analog input pipeline.
TABLE I
TCCAMU PERFORMANCE SUMMARY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL (typical)</td>
<td>&lt; 200 ps</td>
</tr>
<tr>
<td>rms INL</td>
<td>90 ps rms</td>
</tr>
<tr>
<td>DNL (typical)</td>
<td>&lt; 35 ps</td>
</tr>
<tr>
<td>rms DNL</td>
<td>10 ps rms</td>
</tr>
<tr>
<td>LSB Width</td>
<td>107 ps</td>
</tr>
<tr>
<td>Input Range</td>
<td>16 ms</td>
</tr>
<tr>
<td>Output Range</td>
<td>150 LSB</td>
</tr>
<tr>
<td>Average Power Dissipation (including A/D conversion)</td>
<td>8.28 mW</td>
</tr>
<tr>
<td>Area of TCCAMU</td>
<td>2.0 mm x 2.2 mm</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS 1.2 μm nwell</td>
</tr>
<tr>
<td>Chip to chip gain mismatch</td>
<td>&lt; 0.2 %</td>
</tr>
<tr>
<td>Max pedestal offsets between analog capacitors</td>
<td>&lt; 8 LSBs</td>
</tr>
<tr>
<td>Input Referred Random Noise (quantization + jitter)</td>
<td>40 ps rms</td>
</tr>
</tbody>
</table>

The average power dissipation during A/D conversions is 8.28 mW/channel. A small chip to chip gain mismatch of < 0.2 % was accomplished with the use of a time to charge converter (TCC). Pedestal offsets between any two capacitors within a channel are < 8 LSB's; efforts are underway to reduce these offsets to ~ 1 LSB.

In summary, the TCCAMU's high performance and low power dissipation make it suitable for massively parallel data acquisition systems. By counting the reference clock, the dynamic range can be greatly extended for use in high energy physics experiments.

V. APPENDIX

A. Measurement of the DNL

Finding the DNL (differential nonlinearity) involves measuring the width of each output LSB. The DNL of code “Y” can be expressed as:

\[
DNL_Y = \text{Code Width}_Y - 1 \text{ LSB}. \tag{1}
\]

The width of an output LSB can be found with a code density test. By randomizing the TDC analog input a histogram of the output LSBs can be produced, and from this one can statistically determine the width of each code. The probability distribution for the random inputs is often chosen to be a constant over the entire input range. In our case, however, a Gaussian distribution was used for the code density test. This was easily accomplished by adding a finite amount of jitter to the Discr arrival time in the test setup.

The total jitter \( \sigma_J \) occurring at the TCCAMU output can be written as the sum of the jitters in the Discr, system clock, and the TCCAMU itself:

\[
\sigma_J^2 = \sigma_{\text{Clock}}^2 + \sigma_{\text{Discr}}^2 + \sigma_{\text{TCCAMU}}^2 \tag{2}
\]

The jitter that was added to the Discr was made to dominate the contributions from the Clock and the TCCAMU. In
where the summation is over all possible output codes. Note here that the \( \% \) error in determining \( \sigma_J \) is much smaller than the \( \% \) error in the measurement of a single code width.

The other aspect when making DNL and INL measurements with a Gaussian input signal is to verify that the jitter due to \( \sigma_J \) has a true Gaussian shape (or nearly so). If we refer to (5) and take the derivative \( d/d\gamma_2 \) of both sides, we find that:

\[
d\gamma_1/d\gamma_2 = -1.
\]

(8) tells us that if the total output jitter \( \sigma_J \) is Gaussian, and if we vary the input Discr delay over a small range to get a number of \( (\gamma_1, \gamma_2) \) pairs for a given output code, then these points should all lie on a straight line with a slope of -1. Fig. 12 verifies that we have a Gaussian-shaped jitter to within the measurement error. There were 1000 output samples taken for each data point shown.

C. Measurement Uncertainty in DNL

In order to find the measurement uncertainty in the DNL, we must find the uncertainties in \( \gamma \) and \( Pr \). Let:

- \( N \) = number of input samples generating the Gaussian
- \( Pr \) = measured probability in tail of Gaussian
- \( \sigma_P \) = Std dev of \( Pr \) from the actual probability,
- \( \sigma_1 \) (or \( \sigma_2 \)) = Std dev of measured \( \gamma_1 \) (or \( \gamma_2 \)),
- \( \sigma_{12} \) = Std dev of measured \( \gamma_1 + \gamma_2 \),
- \( \sigma_J \) = total rms jitter at the TCCAMU output,
- \( \sigma_{DNL} \) = measurement uncertainty in the DNL, and
- \( \sigma_{Width} \) = measurement uncertainty in a code width.

Using the binomial distribution to determine how many of the \( N \) inputs actually land in the tail of the Gaussian, we find that:

\[
\sigma_P = \sqrt{Pr(1 - Pr)/N}.
\]

If we now take the derivative \( d/d\gamma \) of both sides of (3) using the Leibnitz Rule, assuming that \( \sigma_P \) is sufficiently small (i.e., \( N \) large), then we can write:

\[
\sigma_1 \approx \sqrt{2\pi \sigma_P \exp(\gamma_2^2/2)}.
\]

Finally, from (5) and (6) we see that:

\[
\sigma_{Width} = \sigma_{DNL} = \sigma_J \sigma_{12} < 2\sigma_J \sigma_1.
\]

For \( N = 1000 \) and \( 0.5 > Pr > 0.05 \), we use (3), (9), and (10) to find that \( \sigma_1 < 0.066 \). In our measurements, we added a jitter to the Discr such that \( \sigma_J \approx 0.6 \) LSB. Using (11) we finally have:

\[
\sigma_{DNL} < 0.079 \text{ LSB} = 8.5 \text{ ps}
\]

Increasing the value of \( N \) will decrease the measurement uncertainties in both the DNL and the code widths.
REFERENCES


Eric J. Gerds (S’88) was born in Mount Vernon, NY, on November 9, 1965. He received the B.S. and M.S. degrees from the Moore School of Electrical Engineering at the University of Pennsylvania, Philadelphia, in 1987 and 1991. He is currently working towards the Ph.D. degree at the Moore School.

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W. Eyckmans photograph and biography not available at time of publication.