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Keywords
corticonic network, cortical patch, nonlinear interconnection

Comments

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A CMOS Monolithic Implementation of a Nonlinear Interconnection Module for a Corticonic Network

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Abstract—A nonlinear interconnection module for a corticonic network is designed and fabricated in a 0.6 \( \mu \)m CMOS process. The module uses NMOS transistors in weak-inversion region for nonlinearity. A calibration scheme is developed to compensate for the process and temperature variation of the circuit. The designed module has an area of 0.35\( \text{mm}^2 \). It consumes 200nW of power, with 5V power supply. Simulation results show that the circuit is able to implement the target parametric coupling function accurately.

I. INTRODUCTION

Macroscopic modelling can pave a way leading to the design of high-performance complex and intelligent systems. Extensive research suggests that cortical column (CC) is the basic functional unit in the cortex. A macroscopic modelling approach for a cortical patch has been proposed in [1]. Inside the network, a group of nonlinear dynamic elements are coupled through nonlinear connections, as shown in Fig. 1. The element is designed in such a way that its individual dynamics conforms to or are similar to that of a CC.

As a further effort, a cortical patch similar to Fig. 1 is implemented in silicon [2]. In an accompanying paper [3], the circuit design of integrated-circuit retaion oscillator neuron (IRON) is presented. The IRONs are able to generate arbitrary one-dimensional map in high resolution.

In order to control and correlate the dynamics of different IRONs, nonlinear parametrical coupling is used in the network [1]. In this paper, the CMOS design of the nonlinear interconnection module is presented. Hspice simulation results are included to show the characteristics of the designed module.

II. PARAMETRICAL COUPLING

The processing element presented in [3] uses a bifurcation parameter \( \mu \) to control the dynamic behavior. The parametrical coupling is a type of nonlinear interconnection that is used to control \( \mu \) whose value depends on its own output and those of other IRONs. The bifurcation parameter for the i-th IRON is controlled by both external and internal influences according to

\[
\mu_i(t) = e^{-\alpha t} g(X_i^e, C_i^e) + \frac{1 - e^{-\alpha t}}{N_i} \sum_{j \in \{N_i\}} g(X_j, C_{ij})
\]  

(1)

Where \( X_i^e \in [0, 1] \) is the i-th IRON’s external input, \( X_j \in [0, 1] \) is the output from the j-th IRON, \( C_i^e \) is the coupling parameter for i-th external input, and \( C_{ij} \) is the coupling parameter from j-th IRON to the i-th IRON.

The first term in Eqn. 1 represents the influence of the external input, while the second term is the average effect from IRONs inside the network. \( e^{-\alpha t} \) is named the forgetting factor (FF), while \( 1 - e^{-\alpha t} \) is denoted as FF. As the network adapts, FF exponentially decreases. As a result, the external influence gradually gives way to internal influence. The \( g() \) function in Eqn. 1 is a nonlinear function, as defined in Eqn. 2, and is plotted in Fig. 2.

\[
g(X, C) = X^C, \quad X \in [0, 1]
\]  

(2)

\( \{N_i\} \) in Eqn. 1 is the group of IRONs connected to the i-th IRON. In our corticonic network, local coupling (LC), consisting of self and nearest neighbors, is used, which sets \( N_i = 3 \). The local interconnection scheme of the i-th IRON in the network is shown in Fig. 3. Hence, the designed corticonic network consists of dozens of processing elements (PE), each of which includes an IRON and an LC module.

III. CIRCUIT DESCRIPTION

The parametrical LC in Eqn. 1 is designed in a 0.6\( \mu \)m CMOS process. The supply voltage is 5V. The block diagram
of the implemented LC is shown in Fig. 4. All the operations are carried out in the voltage domain. \( X \)'s are the firing phases from the IRONs, which lie in the voltage range of [2.8V, 3.2V]. In normal operation, \( X \)'s changes their value with a frequency of 1MHz, as stated in [3]. \( C \)'s are coupling parameters with voltage values in the range of [3.0V, 3.4V]. FF are the same for all the PE's in the network. In our simulations, the decay time constant \( \alpha \) is set to be 10\( \mu \)s. Therefore, FF and FF can be controlled from off-chip through two normal analog pads.

The design of a reliable nonlinear function \( g() \) is central in the LC circuit. The nonlinear \( g() \) function in Eqn. 2 can be decomposed into a series of functions, as shown in Eqn. 3. Hence, it can be implemented as a cascade of stages, consisting of a logarithmic module, a multiplier and an exponential module, as shown in Fig. 5.

\[
g(X, C) = X^C = \exp(C \times \log(X))
\]  

(3)

**A. Logarithmic Module**

The circuit of the logarithmic module is shown in Fig. 6. It includes a Gilbert cell and an NMOS M1, which is designed with a large W/L to be biased in the weak inversion region. Without considering the OPAMP offset, using the MOS BSIM3 model in [4], the equation for the Gilbert cell and the NMOS transistor is in Eqn. 4. One can write that

\[
k_{log}V_x V_{ref} = I_{s01}\exp(V_{log} - V_i - V_{off})
\]  

(4)

Where \( k_{log} \) is a coefficient related to transistors in the Gilbert cell. \( I_{s01} \) and \( V_{off} \) are coefficients related to M1. \( V_i \) is the threshold voltage of M1. \( V_t \) is the thermal voltage, \( n \) is the subthreshold slope parameter.

Hence, the output signal of the logarithmic module in Fig. 6 can be derived as shown in Eqn. 5.

\[
V_{log} = V_i + V_{off} + nV_t\log\left(\frac{k_{log}V_x V_r}{I_{s01}}\right)
\]  

(5)

**B. Multiplier**

The voltage multiplier in the \( g() \) module is shown in Fig. 7. It includes two cross-connected Gilbert cells. Again, ignoring the OPAMP offset, the circuit equation for the voltage multiplier in Fig. 7 is shown in Eqn. 6.

\[
k_{ge1}(V_{log} - V_T)V_c = k_{ge2}(V_{dlog} - V_T)V_{cr}
\]  

(6)

Where \( k_{ge1} \) and \( k_{ge2} \) are the transistor related coefficients for the two Gilbert cells. If transistors in the two cells match, the output of the voltage multiplier would be in Eqn. 7.

\[
V_{dlog} = V_T + \frac{V_c}{V_{cr}}(V_{log} - V_T)
\]  

(7)
\[ \frac{V_{\text{logexp}} - V_{o-}}{V_{T}} = \left( \frac{I_{\text{sat}}}{k^V_{T}} \right) \frac{V_{c}}{V_{T}} \] (12)

If the biasing voltage \( V_r \) can be set as in Eqn. 13, the output voltage can be expressed by Eqn. 14.
\[ V_r = \frac{I_{\text{sat}}}{k} \] (13)
\[ V_{\text{logexp}} = V_{o-} - (V_x) \frac{V_{c}}{V_{T}} \] (14)
Therefore, the value of \( C \) in Eqn. 3 is set by \( \frac{V_{c}}{V_{T}} \).

D. Generalized Threshold Calibration

The ideal \( g() \) function in Fig. 2 has two converging points, A and B. Point A represents 0 input. For the circuits in Fig. 6-8, the convergence at point A can be fulfilled relatively easy. However, the convergence at point B is not easy to obtain, because, in reality, it is difficult to set biases to fulfill Eqns. 11 and Eqn. 13. The process parameters on the right side of the equations are not known accurately. Instead, we use a calibration process to resolve this biasing problem.

Let us assume that the differential input signal \( V_x \) varies between 0 and \( V_{\text{inmax}} \). The maximum input can be used to calibrate for point B. The input of the circuit is set to \( V_{\text{inmax}} \) first. Then, the generalized threshold voltage \( V_T \) is adjusted to align the output signal \( V_{\text{logexp}} \) to the converging point B, which means \( V_{\text{logexp}} \) would not change with different \( C \) values, i.e. \( \frac{V_{c}}{V_{T}} \). Thus, using Eqn. 7, we can write \( V_T \) as follows.
\[ V_T = V_i + V_{\text{off}} + n\nu \log \left( \frac{kV_x}{V_{\text{inmax}}} \right) \frac{V_{\text{sat}}}{I_{\text{sat}}} \] (15)

With Eqn. 5, Eqn. 7, Eqn. 9 and Eqn. 15, the output signal from the \( g() \) module can be shown to be in Eqn. 16.
\[ V_{\text{logexp}} - V_{o-} = \left( \frac{V_x}{V_{\text{inmax}}} \right) \frac{V_{c}}{V_{T}} \] (16)

E. Offset Effect

The derivation so far are based on ideal OPAMPs. The OPAMP offset generates current offset between the two branches of PMOS current mirrors, in Fig. 6-8. The current offsets are the most significant systematic error for the module.

If we assume the existence of current offsets \( \Delta I_1 \), \( \Delta I_2 \) and \( \Delta I_3 \) for the three operation modules, using equations similar to Eqn. 4, Eqn. 6 and Eqn. 8, the output voltage can be written as Eqn. 17, under the condition of Eqn. 11.
\[ \frac{V_{\text{logexp}} - V_{o-} + \Delta I_3}{V_{T}} = e^{\frac{\Delta I_2}{kV_{T}}} \frac{V_x + \Delta I_2}{kV_{T}} \frac{V_{c}}{V_{T}} \] (17)

Compared to Eqn. 12, the offset effect is plotted in Fig. 9. The shaded area is the region for ideal \( g() \) function. \( \Delta I_1 \) moves the box along the X axis, \( \Delta I_2 \) moves the box along the \( g \) axis, while \( \Delta I_3 \) stretches the box in \( g() \) direction. Because the weak-inverted NMOSs M1-2 have large W/L size, \( k \) in Eqn. 17 is large. The error \( \frac{\Delta I_1}{kV_{T}} \) and \( \frac{\Delta I_2}{kV_{T}} \) can be designed to be less than 1mV. In our application, their effects can be neglected. The effect of \( \Delta I_2 \) can be compensated by the following FF weighing circuit.
F. Stability

Enhancing the OPAMP gain can effectively reduce the offset level. However, the loops in Fig. 6-8 are susceptible to instability. The feedback loop of the multiplier in Fig. 7 is opened in Fig. 10. Without extra care, the phase margin in the loop can fall short. The feedback loops of Fig. 6 and Fig. 8 are similiar, but with a common source stage. In order to improve the loop phase margin, the OPAMP can be designed to have low gain, or the resistance at the common drain nodes can be lowered. Unfortunately, both methods tend to increase the current offset level in the loop. In our design, we used both methods to guarantee the loop stability under different Spice corner models and temperature variations.

G. FF Weighing Circuit

The FF factors are added by the circuit in Fig. 11. It includes five Gilbert cells for current operation. If all the Gilbert cells match, the output voltage can be expressed as in Eqn. 18.

\[ V_o = \frac{V_{f1}}{V_{fr}} V_{ix1} + \frac{V_{f3}}{V_{fr}} \sum_{i=1}^{3} V_{ixi} \]  \hspace{1cm} (18)

Therefore, FF is set by \( \frac{V_{f1}}{V_{fr}} \) and FF is set by \( \frac{V_{f3}}{V_{fr}} \). Similiar offset analysis shows that the offset in Fig. 11 can be compensated by adjusting \( V_{o-} \).

IV. Simulation Results

The interconnection module is designed and fabricated in a 0.6um CMOS process. The active die area is 970\( \mu \)m \( \times \) 360\( \mu \)m. The power consumption is 200 mW for a 5V supply. The chip is being tested, and results will be available at the time of conference.

The design is fully simulated by Hspice, for different corner models including temperature variations. Loop stability is guaranteed over the full range. The Hspice simulation results of the \( g() \) module, after generalized threshold calibration, with typical Spice models and room temperature, is shown in Fig. 12. The over-streching due to the current offset \( \Delta I_2 \) is less than 5%. It can be compensated by the value of \( \frac{V_{f1}}{V_{fr}} \) and \( \frac{V_{f3}}{V_{fr}} \) in the FF weighing circuit.

V. CONCLUSION

The nonlinear parametrical coupling of a corticonic network is presented. The interconnection module is used to control and coordinate the dynamics of bifurcating neurons in the network. The circuit is implemented and fabricated in a 0.6um CMOS process. The circuit uses NMOS in weak-inversion for nonlinear operation. The designed circuit employs a calibration scheme to compensate process variation and temperature variation for the circuit, especially for the weak-inverted NMOS.

REFERENCES