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Abstract

Least-Mean-Squares (LMS) based mixed-signal scheme for self-calibration of pipelined Analog-Digital Converter (ADC) is proposed. The technique uses an elegant continuous reference update algorithm to correct for gain errors and offset errors in a pipeline stage with minimal area and power overhead. Simulation results show the effeciency of the scheme for resolution of greater than 13bits in a CMOS process.

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Abstract— **Least-Mean-Squares(LMS) based mixed-signal scheme for self-calibration of pipelined Analog-Digital Converter (ADC) is proposed. The technique uses an elegant continuous reference update algorithm to correct for gain errors and offset errors in a pipeline stage with minimal area and power overhead. Simulation results show the effeciency of the scheme for resolution of greater than 13bits in a CMOS process.**

I. Introduction

Pipelined Analog-to-Digital Converters(ADC) architectures are very popular in the design of high-resolution and high-speed ADCs used in broadband communication systems. One such application is a design of a direct conversion receiver, where a high performance ADC enables multi-mode functionality capable of supporting various communication standards, thereby lowering system cost. However, ADCs designed in digital CMOS technology for reasons of low-cost and higher integration do not offer high resolution because of poor capacitor matching, low amplifier gains attributed to lowering supply voltages, charge injection errors, offset errors and poor noise performance. In such cases, self-calibration is always used to push the resolution performance of the ADC [1],[2],[3],[4]. All these calibration schemes mostly correct for errors only due to poor capacitor matching. However they fail to account for the finite gain error of the operational amplifier which has become common-place in today's CMOS technologies with lowering supply voltages. Recently a few digital calibration schemes based on Least-Mean-Squares(LMS) technique have been proposed to correct for errors introduced by finite amplifier gain and capacitor ratio mismtach in a pipeline stage [5],[7]. However these schemes require complex digital processing hardware and do not render itself to easy system on chip implementations. Some of these schemes even need a separate calibration signal added to the input which sacrifices the converter's useful dynamic range [7]. This paper describes an improved mixed-signal calibration scheme for a pipelined ADC using an LMS based adaptive reference-update algorithm which does not have aforementioned drawbacks.

II. One-Bit Per Stage Pipeline A/D Converter

A simplified block diagram of a conventional 1-bit per stage, pipelined ADC is shown in the figure 1. It consists of a sample-and-hold amplifier, a coarse ADC, a coarse DAC and a gain stage. The most significant bits are resolved by

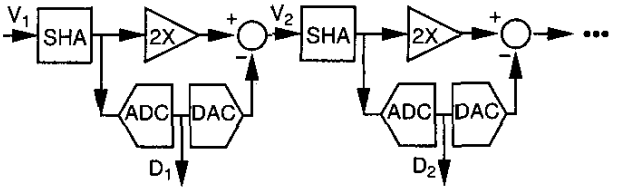

Fig. 1. N-stage 1-bit per stage pipelined ADC prototype

the stages earlier in the pipeline and the least significant bits are resolved later in the pipeline. The most favorable reason for the use of the pipelined ADC for high speed applications is that it's complexity scales linearly with the resolution of the converter (compared to Flash type converters). Since most significant bits are resolved in earlier stages, the overall resolution of the ADC is mostly limited by the first few stages in the pipeline. To understand the sources of error in a pipeline stage, consider a most conventional switched capacitor implementation as shown in figure 2. A single ended circuit is shown for simplicity. V_{refp} is the positive reference voltage and V_{refn} is a negative reference voltage ($V_{refp} = -V_{refn} = V_{ref}$). The resolvable input range of the converter is given by $2V_{ref}$. Each stage consists of

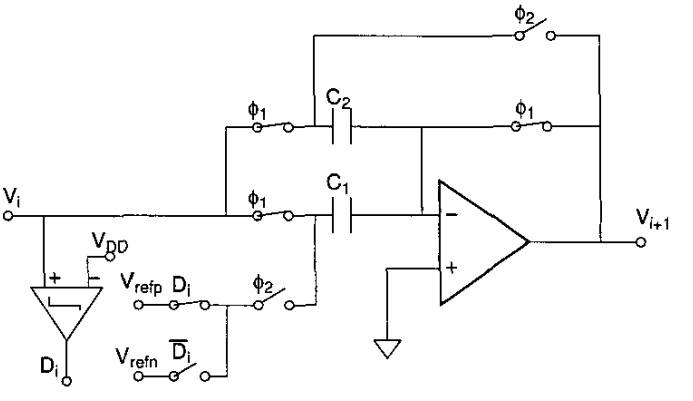

Fig. 2. Switched capacitor 1-bit pipeline stage

two nominally equal capacitors C_1 and C_2, an operational amplifier(op-amp), and a comparator. During the sampling phase ϕ_1, the comparator produces a digital output D_i:

$$D_i = \begin{cases} 1 & \text{if } V(i) \geq V_{th} \\ -1 & \text{if } V(i) < V_{th} \end{cases} \quad (1)$$

where, $V_{th}(=0)$ is the threshold voltage defined midway between V_{refp} and V_{refn}. the bipolar representation of D_i is used for notational convenience. During the multiply-by-2 and subtract phase, the above circuit generates a residue voltage output V_{i+1} given by:

$$V_{i+1} = K\left[\left(1+\frac{C_1}{C_2}\right)V_i + \frac{C_1}{C_2}D_i V_{ref}\right] \quad (2)$$

$$K = \frac{A_0}{1+\frac{C_1}{C_2}+A_0} \quad (3)$$

where, the parameter K is an op-amp gain error coeffecient (ideally unity) and A_0 is the finite op-amp gain. This output residue voltage is then passed to the next stage $i+1$, and the same operation continues. As evident from the above expression, the accuracy of the overall converter depends on the accuracy of the residue output generated by pipeline stages (especially early in the pipeline). Ideally, we expect the residue output voltage to be:

$$V_{i+1} = 2V_i - D_i V_{ref} \quad (4)$$

From expression 3 and 4, we see that gain errors are introuduced in the overall transfer chracteristic because of the term K attributed to finite amplifier gain and the term $\frac{C_1}{C_2}$ which deviates from the ideal value of 1 due to poor capacitor matching. This usually limits the overall resolution of the ADC to 8-10 bits without calibration in today's CMOS process. Charge injection errors have been neglected, since they can be easily corrected through the use of bottom-plate sampling technique and differential operation.

III. Basic Idea of the Proposed Scheme

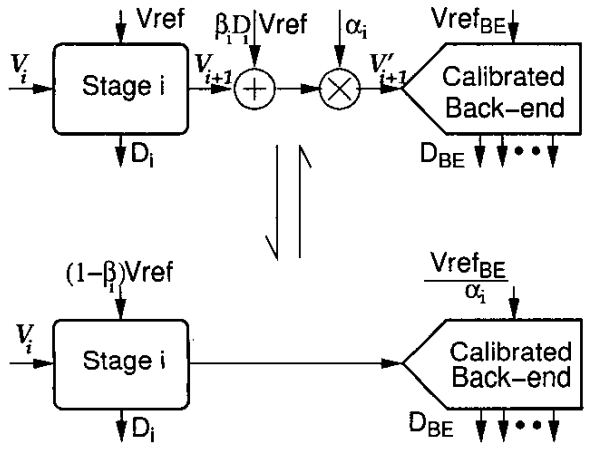

Fig. 3. Basic principle of mixed signal calibration through equivalence of analog processing and the proposed reference manipulation scheme

To correct for gain errors introduced in the pipeline, the residue output of each non-ideal stage in the pipeline can be processed in an analog domain using a set of parameters (α_i, β_i) for each stage i that essentially perform linear translation of the residue output.

$$V_{i+1} \rightarrow V'_{i+1} = \alpha_i\,(V_{i+1} + \beta_i D_i V_{ref})$$

This principle is illustrated in the figure 3. The stage i is the i^{th} stage of the pipeline which is under correction and the $Back-end$ refers to the following stages in the pipeline. If the value of α_i, β_i for stage i can be set as following, then the modified residue output V_{i+1} will resemble the ideal residue output.

$$\alpha_i = \frac{2}{K(1+\frac{C_1}{C_2})}, \quad \beta_i = \frac{K}{2}\left(\frac{C_1}{C_2}-1\right) \quad (5)$$

A digital scheme using a slow but high resolution ADC (SHADC) to estimate these parameters alongwith digital post processing was shown by the same authors [5] [6]. In that implementation, a slow high-resolution ADC was used to perform parameter estimation of the correction parameters α_i, β_i. One of the critical problems with such an implementation was the dependence of the accuracy of calibration on the performance of the SHADC. Also, the technique needed high speed multipliers to perform error compensation in digital domain.

A direct analog scheme as shown in top section of the figure 3 will be difficult to implement due to speed and power constraints. The basic idea of this paper is to perform error compensation in analog domain through manipulation of reference voltages to each pipeline stage. The process of multiplying a residue output by a gain term α_i can be shown to be equivalent to scaling the reference voltages of all the following pipeline stages by $1/\alpha_i$ [4]. Similarly the process of adding an offset term $\beta_i D_i V_{ref}$ to the residue output can be shown to be equivalent to adding a term $-\beta_i V_{ref}$ to the the reference voltage of the stage under correction. This equivalence is illustrated in the figure 3.

The parameter estimation process for α_i, β_i could be performed using the scheme proposed in [5] which requires a use of an SHADC. However, to reduce power consumption, and taking notice of the fact that in most applications, an ADC is not being used constantly, the use of an additional complex converter with higher accuracy is not justified. Hence a mixed signal scheme with an elegant novel reference update algorithm has been proposed which performs parameter estimation during start-up and/or when the ADC is *idle*.

IV. Complete Mixed-Signal Implementation of the Calibration Scheme

Figure 4 shows the reference update scheme for the stage i, that needs calibration. The technique uses a low-resolution, monotonic DAC (CDAC), that behaves like a digital potentiometer around a nominal reference value, to provide reference input to the pipeline stages. During the *inactive or idle* mode of the ADC, the input to the stage i is forced to either fullscale $V_{ref}, -V_{ref}$ or ground. For

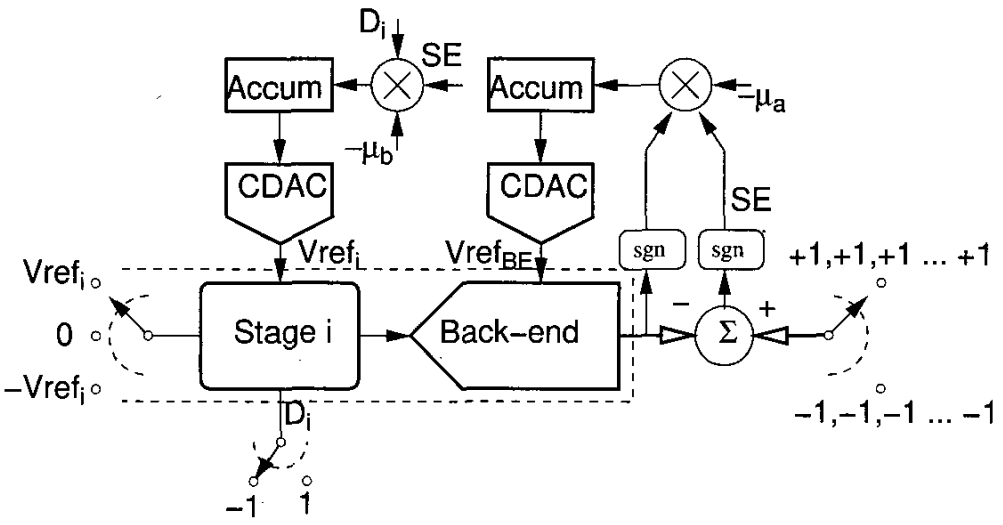

Fig. 4. Mixed Signal Implementation of the Calibration Scheme

the grounded input, the digital output of the stage is also forced to either $D_i = 1$ or $D_i = -1$. This generates a total of four different *known* input values to the stage i. For each of these four input values, the only possible set of outputs from the following pipeline stages (shown as a block $Back - end$ in the figure 4) in an ideal situation is either all 1's $+1, +1, +1... + 1$ or all -1's $-1, -1, -1... - 1$. Any deviation from the ideal values of the back-end suggests gain and offset error for the pipeline stages i onwards.

A sign-sign LMS algorithm is used to continuously updates the reference voltage $Vref_{BE}$ for the back-end and the reference voltage $Vref_i$ of the stage i under calibration by randomly or sequentially switching the inputs to the suggested four input configurations. Let the sign of the deviation of the digital output of the back-end from it's ideal value be given by the SE, as shown in the figure 4. The update algorithm for $Vref_{BE}$ and $Vref_i$ at time index n is given below:

$$\begin{aligned} Vref_{BE}[n] = &\quad Vref_{BE}[n-1] - \mu_a \;\; SE \;\; sgn(D_{BE}) \\ Vref_i[n] = &\quad Vref_i[n-1] - \mu_b \;\; SE \;\; D_i \end{aligned} \tag{6}$$

μ_a and μ_b are the update sizes for the above sign-sign update algorithm. Their value is chosen as small as possible, considering the signal and quantization noise power constraints, the excess mean squared error bounds and the convergence accuracy. The step size can be made programmable for faster convergence [6]. For reasons mentioned in section II, only the first few stages of the pipeline will need calibration. Once the parameters for the stage i are estimated, similar estimation can be carried out for stage $i - 1$ and so on. A recursive estimation process beginning with the least significant Bit(LSB) stage that needs calibration until the Most Significant Bit (MSB) stage is ideal for estimation purposes since the $Back - end$ would resemble an ideal converter for the given accuracy. The error term in Eq.6 now corresponds to only the error contribution from stage i. To increase the accuracy of the scheme, however, the quantization noise power in D_{BE} needs to be reduced. This can be achieved by using a few extra pipeline stages towards the end of the ADC.

The CDAC in the figure 4 should be monotonic over the possible input range. The linearity of CDAC is not critical, since the update loop automatically accounts for the non-linearity of this DAC. The resolution of the DAC may be small of the order of 6-8 bits with monotonicity equal to the overall resolution of the converter. This low-resolution, mononic potentiometer DAC can be easily implemented using current steering thermometer-decoded arrays [8], which guarantees inherent monotonicity and small step sizes. The power consumption of such a DAC is indeed very small and would only be a small percentage of the overall power consumption pie. Further power savings can be achieved by sharing the CDAC between adjacent stages of the pipeline. The multiplication operation in the figure 4 is merely an addition or subtraction operation by a value of μ_a (or μ_b) depending on the polarity of the other inputs (SE, D_i and D_{BE}). Hence the overall calibration loop only needs an accumulator, adder and a few gates for its implementation.

Compared to the digital post-processing implementation scheme proposed in [5], this scheme does not require any post processing of the raw output, since the digital output of the back-end is already a corrected version. Thus the need for high speed multipliers and adders have been eliminated. This also significantly reduces the digital switching noise coupled to the analog section of the chip.

In the above discussion, we have neglected the input dependence of the non-idealities like the finite op-amp gain. High linearity from amplifiers can be easily obtained by trading the absolute value of the gain for linearity in the design. As indicated from the algorithm, the absolute value of

the gain of the amplifiers is a non-issue within limits imposed by the common mode rejection and other constraints. Some of the other not-so serious non-idealities like comparator offsets and op-amp offsets can be minimized using bottom-plate sampling, differential operation and comparator redundancy in the pipeline stage [3][9].

V. Simulation Results

A 13-bit resolution ADC (intended to run at 100 MHz) is simulated at a behavioral level. There are 16 stages in the pipeline. The technology is assumed to have a capacitor ratio mismatch of 1-3% and the op-amp gain in the range of 800-1200. Pipelined ADC desgined without calibration in such a technology would yield only 8bit resolution even at low speed. In the simulation setup, the CDAC of the figure 4 is assumed to have a resolution of 8 bits with step-size of 14 bit resolution. Since the technology yields raw resolution of 8 bit, only first 5 stages of the pipeline will need calibration to generate an output of 13 bit resolution. As suggested in the proposed scheme, the ADC is calibrated during an *inactive or idle* mode by switching the input of the ADC randomly to assume one of the four input configurations (see section IV) and running the update algorithm before convergence is reached. The figure 5 shows that the Integral Non-Linearity (INL) of the pipelined ADC has improved from a value of ± 64LSB to ± 0.5 LSB. The Differential Non-Linearity (DNL) plot of the figure6(a) indicates that DNL has improved by around 252LSBs.

Figure 6(b) shows the normalized value of the reference voltages for the sixteen stages of the pipeline before and after running the the reference update algorithm. The dashed line indicates the normalized value before calibration.

VI. Conclusion

A mixed signal scheme consisting of a digital reference-update algorithm and an analog error-compensation scheme through manipulation of reference voltage is suggested. The scheme does so with mininmal analog and digital overhead making it suitable for embedded applications. The simulation results for a 13 bit converter has been shown. The results indicate significant improvement in the integral and differential linearity performance of the ADC.

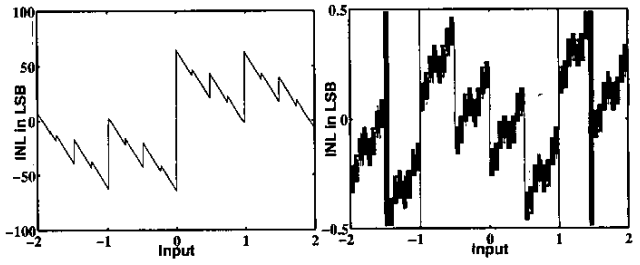

Fig. 5. INL error profile: capacitor ratio mismatch 1-3%, op-amp gain 800-1200 a) Before and b) After Calibration

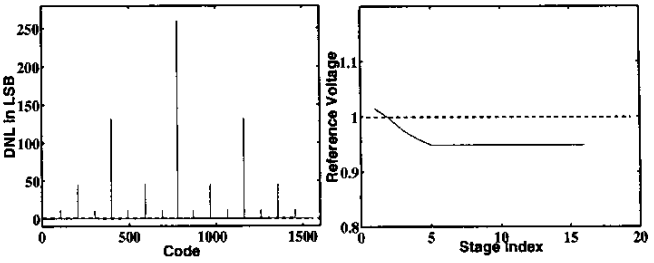

Fig. 6. a) DNL error profile before Calibration (the darker line at 0 shows DNL after calibration) b) The Reference values before (dotted line) and after (dark line) calibration

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