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Low-Power Reduced Transistor Image Sensor

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Abstract
An image sensor comprising an array of 128 by 50 super pixels, column parallel current conveyors and global difference double sampling (DDS) unit is presented. The super pixel consists of: a reset transistor, a readout transistor, four transfer transistors and four photodiodes. The photo pixel address switch is placed outside the pixel, effectively implementing 1.5 transistors per pixel using a sharing scheme of the readout and reset transistor. The column FPN of 0.43% from saturated level and SNR of 43.9 dB is measured. The total power consumption is 5 mW at 30 frame/s.

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Introduction: Low-power CMOS image sensors are used in various applications, including cell phones, security cameras and automotive cameras. Consumer demands for high pixel count imaging sensors have set trends for small pixel pitch sensors, high signal-to-noise ratios, high dynamic range and better colour replication of the imaged scene, among others. State-of-the-art CMOS imaging sensors are based on the voltage mode three-transistor active pixel sensor paradigm [1]. The introduction of correlated double sampling, i.e. focal plane noise suppression, pinned photodiode and low power consumption, has enabled CMOS imaging sensors to close the performance gap when compared to CCD image sensors. Current mode CMOS image sensors have provided an alternative for low power imaging applications. Some of the strongholds for current mode imaging sensors have higher frame rates than voltage mode counterparts [2] and information extraction at the sensory level [3, 4]. The main limiting factors in current mode image sensors have been low image quality owing to the large fixed pattern noise (FPN) and large temporal noise.

This Letter presents a low-power linear current mode image sensor using 1.5 transistors per pixel. The reduced number of transistors per pixel is due to two factors; first, the address switch transistor is eliminated from the pixel and the access of individual pixels is controlled via manipulating the drain and gate voltages of the in-pixel readout transistor; and secondly, four photodiodes share common reset and readout transistors via four transfer transistors. This new pixel architecture allows for smaller pixel pitch owing to the elimination of the switch transistor and access line. The elimination of the access switch also allows for higher linearity between the output photocurrent and the integrated photo voltage and higher SNR figure compared to 3-T current mode APS. Measurements from the image sensors are presented in this Letter.

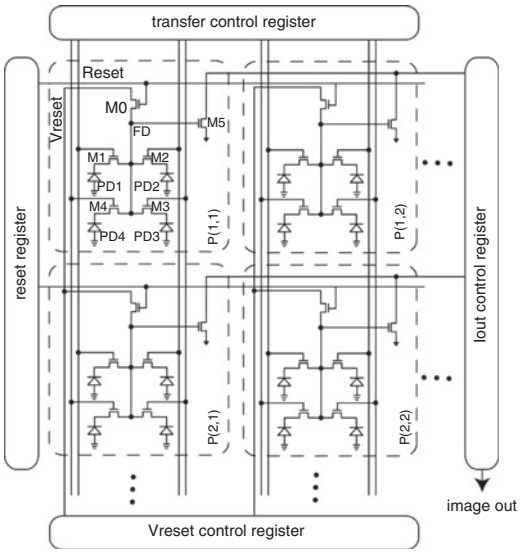

Fig. 1 *Block diagram of 1.5 transistor per pixel image sensor*

Architecture: A high-level block diagram of the image sensor is shown in Fig. 1. The image sensor comprises an array of 128 by 50 super pixels, column parallel current conveyors and global difference double sampling (DDS) unit. Each super pixel consists of: a reset transistor (M0), a readout transistor (M5), four transfer transistors (M1–M4) and four photodiodes. The four photodiodes, PD1–PD4, share a common reset and readout transistor and their access is controlled via transfer transistors M1–M4, respectively.

The access of individual pixels is controlled via manipulating the gate and source voltage of the in-pixel readout transistor M5. To control the gate voltage of the readout transistor, two orthogonal buses are placed in the imaging array. The first bus, which is labelled as Vreset bus, connects the drain nodes of all reset transistors in a column and the second bus, labelled as the Reset bus, which is orthogonal to the Vreset bus, connects the gate nodes of all reset transistors in a row. The column parallel Vreset bus can be set to ground or reset potential of ~3 V via an analogue 2-to-1 multiplexer placed in the periphery of the column. For example, the first Vreset column bus is set to ~3 V and the rest of the column buses are set to ground potential. When the gates of the reset transistors in the first row are set high (5 V), only pixel P(1,1) floating diffusion (FD) node is set to 3 V. The FD node for the rest of the pixels in the first row (P(1,2), P(1,3) etc.) are set to ground potential. Therefore, only pixel P(1,1) readout transistor has a gate voltage above the threshold, i.e. $V_{gs} > V_{th}$, and pixel P(1,1) conducts a current on the output bus. Pixels P(1,2) to P(1,N) are turned off since the FD node is set to ground potential, i.e. $V_g < V_{th}$, and they do not contribute to the output current. The drain nodes of all readout transistors in a row are tied together and connected to a row parallel analogue 4-to-1 multiplexer. The multiplexer allows for a row output bus to be connected to a precharge potential (~0.4 V), a current conveyor that pins the drain potential to ~0.4 V or to ground potential. For example, the output current bus for the first row is connected directly to the current conveyor, while the next row is precharged to 0.4 V in order to speed up access time. Since only pixel P(1,1) in the first row has a gate voltage of the readout transistor above the threshold, pixel P(1,1) output current has access to the current conveyor. The rest of the rows are connected to ground and the drain voltage of the readout transistors is set to 0 V. Therefore, the rest of the pixels in the first column are turned off owing to drain–source potential of 0 V, and the power consumption of the image sensor is minimised.

Results: A prototype of the proposed image sensor was fabricated in a standard 0.5 μm CMOS process. The linearity of the measured output photocurrent from one photodiode of the pixel with respect to time, i.e. integrated photodiode voltage, is measured and shown in Fig. 2. The pixel current is recorded during an integration period of 33 ms. The photodiode discharges by 1.3 V during the integration period and the output current changes from 4 μA of reset current to 1 μA of final signal current. The readout transistor M5 operates in the linear mode for the entire integration period. The right axis in Fig. 2 presents the nonlinearity of the output current computed as a ratio of the residuals (deviations from the linear fit) to the maximum value. The linearity of the output current is better than 99% during the entire integration period. The improved linearity of the output current is due to minimising the column switch impedance, which is placed outside the pixel and low input impedance of the current conveyor. The estimated total impedance along the signal path of the current is ~300 Ω, which is due to the input impedance of the current conveyor and the switch impedance for the analogue multiplexer.

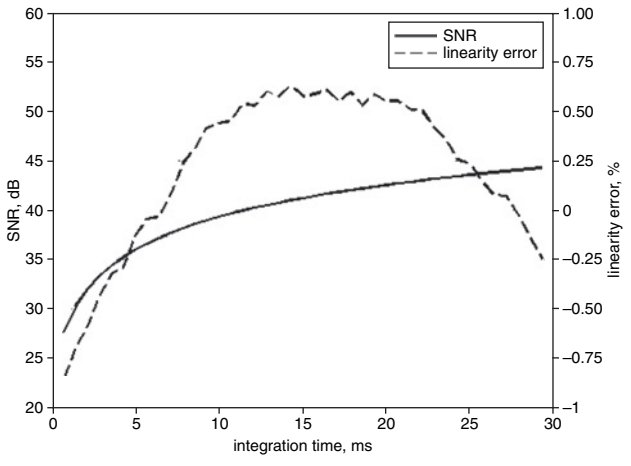

Fig. 2 *Pixel current output against deviations from linear fit*

The left axis in Fig. 2 presents the measured SNR as a function of integration period and constant light intensity of 1 μW/cm2. For short integration periods, the image sensor is limited by the readout circuitry temporal noise, which consists of the thermal noise of the readout transistor, thermal noise of the current conveyor and reset noise owing to transistor M0. For long integration periods, the dominant noise source is the photon shot noise of the photodiode, and the readout circuitry temporal noise has smaller contributions to the final noise. For room light intensity and 30 ms of integration, the SNR for this image sensor is 43.9 dB compared to 39 dB for a 3-T current mode APS [5].

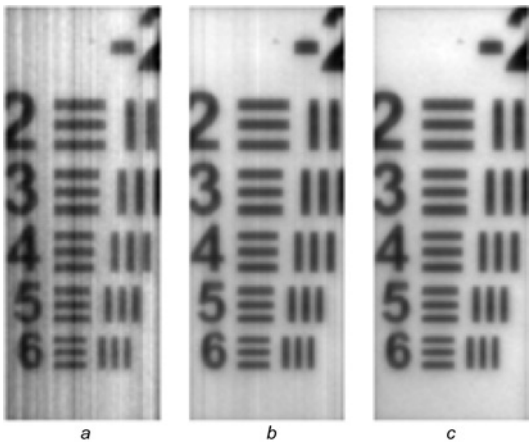

Fig. 3 *Sample images obtained from image sensor*

a Uncorrected image
b On-chip DDS image correction
c Off-chip per row calibration correction

Fig. 3 shows sample images obtained from the image sensors. Fig. 3*a* presents the original image obtained directly from the image sensors without any noise suppression. In this image, large variations across the entire image, as well as row variations, are observed and the features of the image are very difficult to observe. The image in Fig. 3*b* is obtained after the DDS operation. In this image, large variations across different rows are still visible owing to the mismatches between row-parallel current conveyors. In the image in Fig. 3*c*, off-chip row calibration scheme is applied. The row spatial variations are minimised and the spatial noise improvements are clearly evident. The measured FPN figure is 0.43% from saturation level.

Table 1: Summary of image sensor

Technology	0.5 μm Nwell CMOS
Array size for 1.5T image sensor	100 × 256
Pixel size (fill factor)	9 × 9 μm (46%)
FPN with(out) DDS row (entire)	0.43% (2.6%) of sat.
FPN after per pixel gain correction	0.1% of sat. level
Measured input referred noise	3.2 mV
SNR (measured)	43.9 dB
Power consumption	5 mW

Conclusions: We present a low-power linear current mode image sensor. The image sensor is summarised in Table 1. The low fix pattern noise of 0.43% from the saturation value and SNR of 43.9 dB is comparable to voltage mode APS, and the image sensor can be used as a front end for many current mode computational image sensors. Off-chip calibration can further reduce the spatial variations to 0.1% from the saturation value, which is possible because of the high linearity between the output current and integrated photo voltage. The low-power consumption of this system of 5 mW at 30 is another advantage of current mode image sensors.

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