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A CMOS Linear Voltage/Current Dual-Mode Imager

Zheng Yang
University of Pennsylvania

Viktor Gruev
University of Pennsylvania, vgruev@seas.upenn.edu

Jan Van der Spiegel
University of Pennsylvania, jan@seas.upenn.edu

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Abstract
We present a CMOS image sensor capable of both voltage- and current-mode operations. Each pixel on the image has a single transistor acting as either source follower for voltage readout, or transconductor for current readout. The two modes share the same readout lines, but have their own correlated double sampling (CDS) units for noise suppression. We also propose a novel current-mode readout technique using a velocity saturated short-channel transistor, which achieves high linearity. The 300x200 image array is a mixture of 3 types of pixels with identical photodiodes and access switches; while the readout transistors are sized for their designated mode of operation. This ensures a fair comparison on the performance of the different modes.

Keywords
CMOS imager, Image sensor, current-mode, voltage-mode image sensor

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Zheng Yang, Viktor Gruev and Jan Van der Spiegel
Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, PA 19104

***Abstract*— We present a CMOS image sensor capable of both voltage- and current-mode operations. Each pixel on the imager has a single transistor acting as either source follower for voltage readout, or transconductor for current readout. The two modes share the same readout lines, but have their own correlated double sampling (CDS) units for noise suppression. We also propose a novel current-mode readout technique using a velocity-saturated short-channel transistor, which achieves high linearity. The 300x200 image array is a mixture of 3 types of pixels with identical photodiodes and access switches; while the readout transistors are sized for their designated mode of operation. This ensures a fair comparison on the performance of the different modes.**

I. Introduction

CMOS active pixel sensors (APS) incorporate either voltage- or current-mode readout. Voltage-mode readout has been in use since the first 3-transistor (3T) CMOS APS imager [1], and is still the dominant choice of CMOS imagers in market today [2]. Current-mode readout is used mostly to facilitate focal-plane image processing, because many analog computations can be easily done in the current domain [3]. Despite this advantage, most current-mode imagers suffer from higher noise level, or poorer image quality [1].

In the first part of this paper, we report a dual-mode imager architecture that is capable of *both* voltage-mode and current-mode readout. The entire pixel array can be set up in either mode by switches outside the array. Having a unified layout and access scheme, we are able to mix pixels with different readout transistors (but otherwise identical) together in the same array, to establish a fair comparison of their performance in the two operating modes. One CDS unit is included for each mode and shared by all the pixels to reduce fixed pattern noise (FPN). Their working principles are explained in brief.

For efficient noise suppression, linear readout of the accumulated photo charge is required. Linear voltage readout is usually done by a source follower in each pixel that drives the output line. On the other hand, linear current readout makes use of a transconductor, conventionally implemented by a transistor with fixed V_{DS} operating in the linear region [4]. In the second part of this paper, we present a novel technique of linear current readout using a velocity-saturated short-channel transistor. The linearity of a special pixel employing this new technique, as well as its design criteria, are compared with the other two conventional pixels. The 3 types of pixels each makes up $1/3$ of the imager's 300×200 pixel array.

The imager was designed in a standard 0.5μm 3M2P CMOS process, and measures $3\times4.5\text{mm}^2$. It has been fabricated through MOSIS. Simulation results showing the operation of the imager are presented in this paper.

II. Dual-mode Readout Architecture

Fig. 1 shows one pixel in the imaging array with its readout circuitry. The pixel is based on the classical 3T APS design [2]. It includes a photodiode, a readout transistor $M1$, a reset switch $M2$ and a column selection switch $M3$. An additional transistor, $M4$, is used to be able to reset the pixels individually. It implements an AND function such that the reset pulse, which is common to a row, only triggers the reset in the selected column. Likewise, a row selection switch exists at the end of every row of pixels. The row switches, together with the column switches in the pixels, enable the random access of any pixel in the array.

In voltage-mode readout, the mode selection switches are set to position 1. This connects the drain on every readout transistor to VDD. The source, on the other hand, is connected to a constant current bias I_1, for the selected pixel. Accumulated photocharge is detected using the readout transistor as a source follower, in order to drive the readout line associated with a large capacitance. The output circuitry include a voltage-mode CDS for FPN suppression, and an output buffer.

Current-mode operation corresponds to position 2 on the mode selection switches. In this mode, the common terminals of the readout transistors are connected to ground, while the readout line connects to a current conveyor which masks its large capacitance [3]. Under specific bias conditions, the readout transistor in the selected pixel operates as a transconductor. It converts the photocharge linearly to its drain current, which is then copied by the current conveyor and processed by the CDS. Note that the drain and source of $M1$ have exchanged roles in this mode, and readout current now flows *into* the pixel array. The current source I_1 merely adds a constant offset current to meet the input range of the CDS.

III. Noise Suppression Circuits

The imager has one voltage-mode and one current-mode CDS unit. They are shared by all the pixels, thus avoiding mismatch errors introduced with other row- or column-based CDS approaches.

A. Voltage-mode CDS

The voltage-mode readout circuit is shown in Fig. 2. The CDS function is performed by a simple switched capacitor voltage memory. During the first half of the read operation, the switch s is closed. Assuming an ideal current sink I_1, we can approximate the output of the source follower as

$$V_{pixel} = V_{photo} - V_t \tag{1}$$

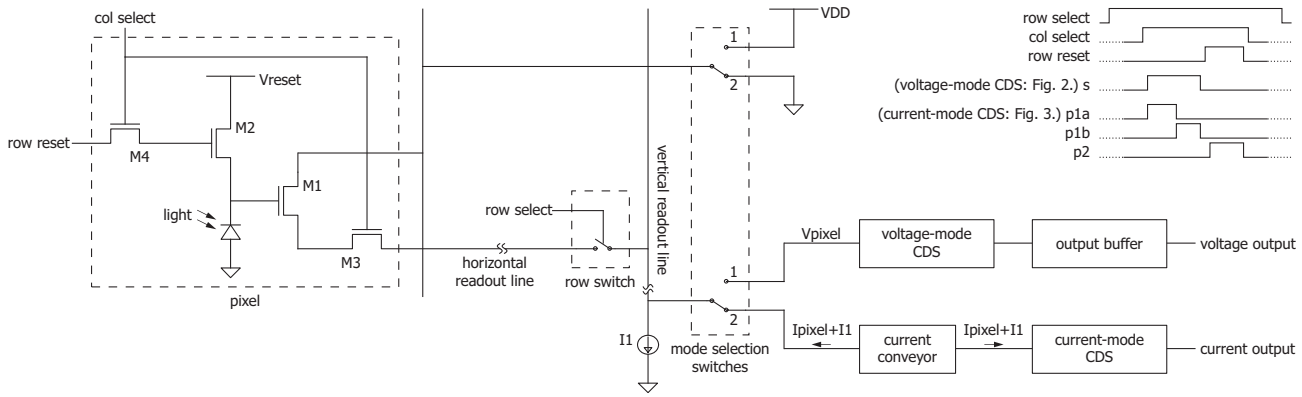

Fig. 1. Pixel schematics and dual-mode readout architecture.

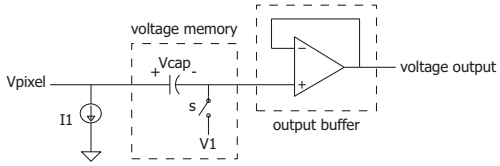

Fig. 2. Voltage-mode readout circuit: CDS and output buffer.

where V_{photo} is the gate voltage of $M1$ at the end of charge accumulation, V_t is the threshold of $M1$. In this phase, the voltage drop across the capacitor is

$$V_{cap} = V_{photo} - V_t - V_1 \tag{2}$$

where V_1 is a constant voltage used to adjust the output range of the CDS. Next, the switch s is open, and the gate of $M1$ is reset to V_{reset} (Fig. 1). Since the capacitor maintains the same voltage drop V_{cap}, the output of the voltage memory must be $(V_{reset} - V_t) - V_{cap}$, or

$$V_{out} = V_{reset} - V_{photo} + V_1 \tag{3}$$

As V_t is cancelled out in the equation, the FPN caused by V_t variation among pixels will be corrected.

B. Current-mode CDS

Fig. 3 shows the current-mode readout circuit. The two current memory cells implement the CDS function, while the current conveyor has two purposes: it clamps the voltage on the readout line to V_{d_ref}, and it passes a copy of the input current $(I_{pixel} + I_1)$ to the CDS. Since the readout line connects to the drain of a readout transistor, whose source is grounded, we can choose a small V_{d_ref} to bias the device in the linear region. In this case, the pixel current is

$$I_{pixel} = \beta[(V_{photo} - V_t) - \frac{V_{d\_ref}}{2}]V_{d\_ref} \tag{4}$$

This current goes to the two-stage current memory, which is based on the S^3I design in [5]. During the $p1a$ phase, the first memory cell is active. The opamp in negative feedback loop sets the gate voltage on $M5$, such that the I_{DS} of $M5$ is equal to $I_{pixel} + I_1$. Then, the $p1a$ switches are open. At this instance, the gate voltage of $M5$ is lowered due to negative-charge injection (since N-channel switches are used). $M5$ now sinks $I_{pixel} + I_1 - I_{e1}$. I_{e1}, representing the error of the first stage, will be memorized by the second stage during the $p1b$ phase. At the end of the phase, the second stage again introduces its error I_{e2}, which becomes the total error of the CDS. However, I_{e2} is only dependent on I_{e1}; it is not directly related to the original value of I_{pixel}. Therefore it can be regarded as a relatively constant offset error, with only a small variance compared to I_{e1} and I_{pixel}.

When the pixel is reset, the expression of pixel current (4) would have its V_{photo} replaced by V_{reset}. The final output in phase $p2$ is then the difference of the two pixel currents, plus the error I_{e2}, i.e.

$$I_{out} = \beta[(V_{reset} - V_{photo})]V_{d\_ref} + I_{e2} \tag{5}$$

Again, V_t is cancelled out, achieving FPN suppression.

The opamps in the memory cells bring an additional benefit, as they fix the drain voltage of $M5$ and $M6$ to V_{o_ref} during memorization. This eliminates the channel length modulation caused by V_D variation. In our actual design, both $M5$ and $M6$ are replaced by cascode devices, making them less sensitive to V_D during the output phase ($p2$). Also, the two opamps are combined into a single one, shared by both cells.

IV. Novel Linear Current Readout Technique

The conventional linear current readout method, as described in section III-B, suffers from two sources of nonlinearity. The first is due to mobility dependence on the gate voltage of the readout transistor, also known as mobility degradation. In other words, the β in (4) becomes a function of V_{photo}. The second is due to voltage drop across the access switches. Although the current conveyor clamps the voltage on the readout line, the V_{DS} across the row and column switches are still function of I_{photo}. This effect is more severe at the in-pixel switch, whose size cannot be very large. As a result, the V_D of the readout transistor can no longer be represented by the constant V_{d_ref} in (4).

Our new technique is immune to the above two causes of nonlinearity. We propose to use a short-channel device working in the velocity-saturated region as the readout transistor.

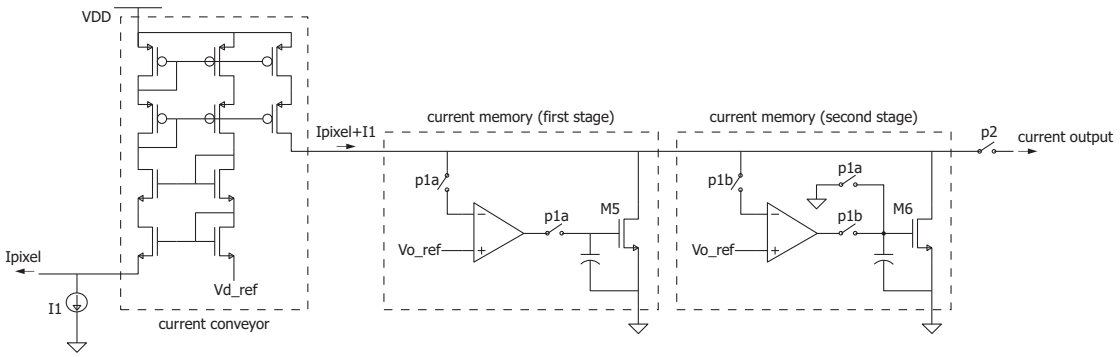

Fig. 3. Current-mode readout circuit: current conveyor and CDS.

Velocity saturation occurs when the electric field along the channel increases beyond a critical value, so that a constant mobility μ_n cannot be sustained. This critical value E_{sat} is about 1.5×10^4 V/cm for p-type silicon [6]. The carrier velocity v_n, normally expressed as $-\mu_n\frac{dV}{dx}$, now reaches a constant v_{sat}. Any further increase in the E-field can only decrease the mobility, but won't increase the velocity. The channel current expression under this condition is, as a first approximation:

$$I_{DS} = v_{sat}C_{ox}W(V_{GS} - V_{DSAT} - V_t) \tag{6}$$

where V_{DSAT} is the drain-source voltage at which velocity saturation comes into play.

$$V_{DSAT} = \frac{E_{sat}L}{1 + \frac{E_{sat}L}{V_{GS}-V_t}} \tag{7}$$

V_{DSAT} is a function of V_{GS}, which determines the degree of velocity saturation. However, when V_{GS} is large (but not so large as to enter linear region), one can regard V_{DSAT} as a constant equal to $E_{SAT}L$. With this approximation, (6) describes a linear relationship between I_{DS} and V_{GS}. Also, in consistent with the saturation of a long-channel device, I_{DS} does not depend on V_{DS} as the channel is pinched off.

Fig. 4 compares the I-V curves of two current-mode readout transistors. One can identify the effect of mobility degradation in both of them, as the curves bend downwards for large V_{GS}. However, velocity saturation is observed for the short-chanel transistor, identified by the dashed box on the second plot. Despite being linear, this region also has a very high voltage-to-current conversion gain.

The same CDS circuit in section III-B can be used with this readout mode. The voltage reference V_{d_ref} of the current conveyor needs to be large enough to ensure saturation, while a small or zero I_1 is desired because of the already-large pixel current. The final output current is:

$$I_{out} = v_{sat}C_{ox}W(V_{reset} - V_{photo}) + I_{e2} \tag{8}$$

Compared with (5), the new technique not only is insensitive to the signal-dependency of μ_n and V_D , but also corrects for the length mismatches of the readout transistors.

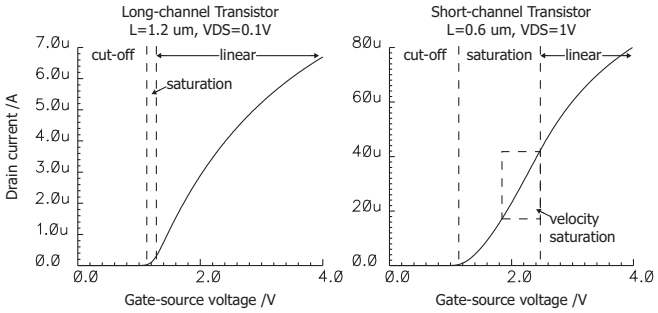

Fig. 4. I-V relationships of two readout transistors with fixed V_{DS}.

V. Transistor Sizing in Pixels

The pixels have a pitch of 12μm$\times12\mu$m and a fill factor of 31.25%. The reset and access switches all have minimum length. $M3$ has the largest width, in order to minimize its on-resistance in current-mode readout. $M2$ has a smaller width in order to reduce the parasitic capacitance at the integrating node, and to limit the charge injection when it switches off from the reset phase. The size of $M2$ and $M4$ were chosen in simulations to ensure that the pixel can be reset in about 100ns in all modes, according to a 30fps output rate. The layout of photodiode and NMOS switches is identical in all pixels.

The final design contains 3 different types of pixels, each has its readout transistor sized for a specific mode of operation. Although it would be convenient to have a universal readout transistor that works in all 3 readout modes, this is however not possible, for the following considerations.

A. Voltage-mode readout transistors

The linearity of the voltage-mode signal path is affected by 3 factors: the readout transistor $M1$'s channel length modulation, body effect, and the current sink I_1's output impedance. When the first two factors are considered, the output voltage of the source follower can be written as [7]:

$$V_S = V_G - V_t - V_{ON} \tag{9}$$

where

$$V_t = V_{t0} + \gamma(\sqrt{|\phi_F| + V_{SB}} - \sqrt{|\phi_F|}) \tag{10}$$

$$V_{ON} = \sqrt{\frac{2I_1}{\beta(1+\lambda V_{DS})}} \tag{11}$$

The two equations describe the body effect and the channel length modulation, respectively. They are both function of the source follower output V_S, which in turn depends on the input voltage V_G. We cannot eliminate body effect with our single well process, however, we can reduce the channel length modulation effect by making β large, i.e. using a large $\frac{W}{L}$. This would make V_{ON} close to zero (which has been assumed in (1)) and less dependent on V_S variation.

The nonlinearity caused by an non-ideal current sink I_1 can be seen by writing out the small-signal voltage gain function of the source follower:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{mbs1} + G_L} = \frac{1}{1 + \frac{g_{mbs1}}{g_{m1}} + \frac{G_L}{g_{m1}}} \qquad (12)$$

where G_L is the total conductance after combining g_{ds1} with the impedance of the load and I_1; g_{m1} and g_{mbs1} are the transconductance and the body transconductance of transistor $M1$, respectively. Since the current sink I_1 has a finite output impedance, its output current I_1 will be a function of V_S. This means that the g_{m1} term in (12) will vary according to the operating point set by V_S, yielding a non-constant gain. To reduce this nonlinearity, g_{m1} must be made large, by choosing a large $\frac{W}{L}$. This also serves to attenuate the body effect, which shows up as g_{mbs1} in the equation.

To summarize, in voltage-mode, $M1$ is required to have a large W and a small L.

B. Current-mode readout transistors in linear region

The sources of nonlinearity in this readout mode have already been discussed in section IV. Mobility degradation is a short-channel effect and can be reduced by choosing a large L. It is also desirable to have a large V_{DS} on $M1$, which makes the voltage drop across access switches less significant. This implies a small $\frac{W}{L}$ for $M1$. In short, this mode requires $M1$ to have a small W and a large L.

C. Current-mode readout transistors in velocity saturation

The onset of velocity saturation requires the E-field along the channel to be greater than E_{sat}. The more this field exceeds E_{sat}, the more it makes V_{DSAT} constant in (6). Therefore it is desirable to have a small L. One may also want to choose a small W to limit the pixel current, in order to match the input range of the current-mode CDS unit, which is also used in the linear-region readout mode. However, making W too small is subject to greater transistor mismatches that won't be corrected by CDS.

VI. Simulation Results

Linearity of the 3 optimized readout transistors were simulated in HSpice, the results are shown in Fig. 5. A DC sweep was performed while the gate voltage of the transistors ramps down by 0.5V, to emulate the accumulation of photocharge. The output levels are normalized to a linear scale between 0 and 1. Linearity is calculated based on the maximum deviation from a best-fit straight line. It is seen that the voltage mode readout transistor yields the best linearity. Velocity-saturated current mode comes a close second, and has a significant improvement over the conventional linear-region current mode.

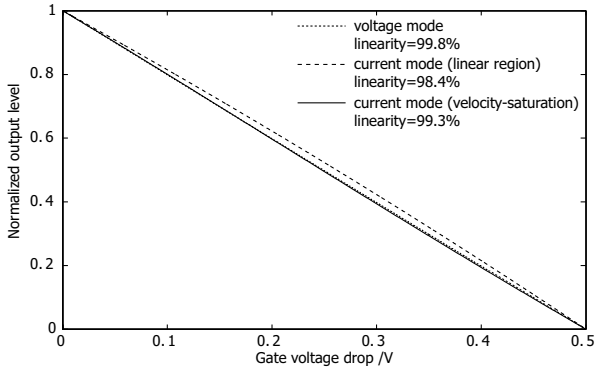

Fig. 5. Normalized output levels of the 3 readout transistors.

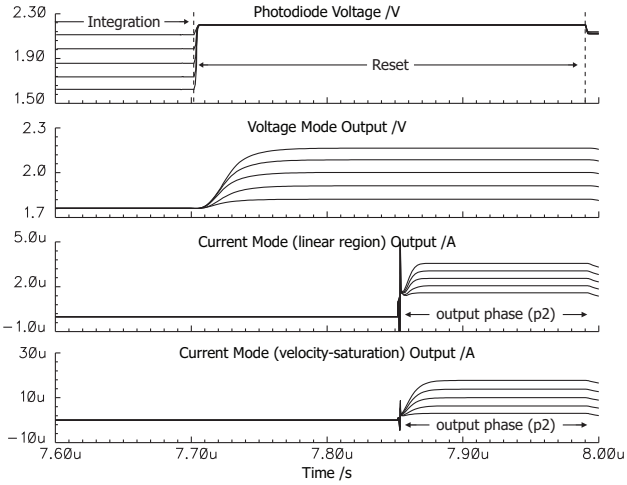

Fig. 6. Output waveforms of the 3 operation modes.

Fig. 6 shows an simulated example of the 3 readout modes at different light intensity. The outputs exhibit linear steps, in accordance with the voltage on the photodiode at the end of a integration cycle.

Acknowledgment

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