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Abstract
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Keywords
CMOS imager, Image sensor, current-mode, current mode image sensor

Comments
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Two Transistor Current Mode Active Pixel Sensor

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***Abstract*—A novel current mode active pixel sensor for high resolution imaging is presented. The photo pixel is composed of a photodiode and two transistors: reset and transconductance amplifier transistor. The switch transistor is moved outside the pixel, allowing for lower pixel pitch and increased linearity of the output photocurrent. The increased linearity of the image sensor has greatly reduced spatial variations across the image after correlated double sampling and the column fix pattern noise is 0.35% of the saturated current. A discussion on theoretical temporal noise limitations of this design is also presented.**

I. Introduction

High resolution imaging is closely related to the number of transistors and line interconnections per pixel. Traditional image sensors have been based on the three transistor active pixel sensor (APS) topology [1]. In order to achieve high resolution imaging, various schemes have been explored where one or more of the three pixel transistors are shared within a neighborhood of pixels and effectively reducing the transistor count per pixel [2]. Other techniques for high resolution imaging have included capacitor and/or BJTs within each pixel in order to control the pixel output or reset phase of the photo diode [3],[4]. A small pitch, high fill factor image sensor was fabricated in a stack 3-D technology, where the photodiode was placed in a top tier and read out circuitry was placed in subsequent tiers [5]. The novel stack 3-D fabrication technology has created new possibilities for high resolution image sensors.

Current mode imaging has been a rival to the more traditional voltage mode APS. Current mode imaging techniques have spun a multitude of sensors, where visual information extraction at the focal plane has been the primary focus and a major stronghold [6]. The limiting factor in current mode imaging sensors has been the low image quality i.e. high fix pattern noise. The primary contributor of fix pattern noise in both voltage and current mode APS is the threshold voltage variations of the read out transistor between pixels in the imaging array. In voltage mode APS, the linear voltage output with respect to the photodiode voltage coupled with correlated double sampling (CDS) circuits allows for suppression of threshold variations between read out transistors in the imaging array [1]. Similar techniques have been employed in current mode imaging [6]. Linear photo current output with respect to photodiode voltage has been achieved by operating the read out transistor of the pixel in linear mode [7]. The linear current output coupled with current conveyers and current mode memory circuits has allowed for high read out speeds (high frame rates) and low FPN figures [6]. One of the factors which have limited the linearity of the current output (hence impacting the FPN figure) has been the finite on resistance of the access transistor in the pixel.

In this paper, we discus a novel imaging sensor based on the linear current mode APS paradigm. The pixel switching transistor has been moved outside the pixel, allowing for an efficient realization of 2 transistors per pixel and effectively reducing the pixel pitch. Furthermore, eliminating the switch transistor from the pixel has allowed for higher linearity between the output photo current and photodiode voltage. The improved linearity has yielded to low FPN figures. The rest of the paper is organized as follows. The pixel schematic and overview of the complete imaging system is presented in Section II. Measurements are presented in Section III and Section IV is dedicated to theoretical temporal noise limits of this design. Concluding remarks are presented in Section V.

II. Pixel Schematic and System Overview

A block diagram of the pixel schematic and the entire image array is presented in Figure 1. The photo pixel is composed of a photodiode, implemented as n-diffusion over p-substrate, and two transistors: a reset transistor M_0 and a transimpedance amplifier M_1. There are five line connections per pixel: power, ground, reset, drain and source line. The key requirement in this imaging architecture is the following: the source and drain lines of the transimpedance amplifier M_1 must be orthogonal to each other. This can be observed in Figure 1, where all pixels in a row (column) connect their drains (sources) to a horizontal (vertical) line. The orthogonal requirement allows for a direct control over the drain-source (V_{ds}) voltage drop across the read out transistor M_1 via the switch transistor M_2. The access of a particular pixel(s) is directly controlled via the drain-source voltage of M_1. If a pixel should be turned on, the V_{ds} is set to a non-zero value. Conversely, if a pixel should be turned off, the V_{ds} is set to

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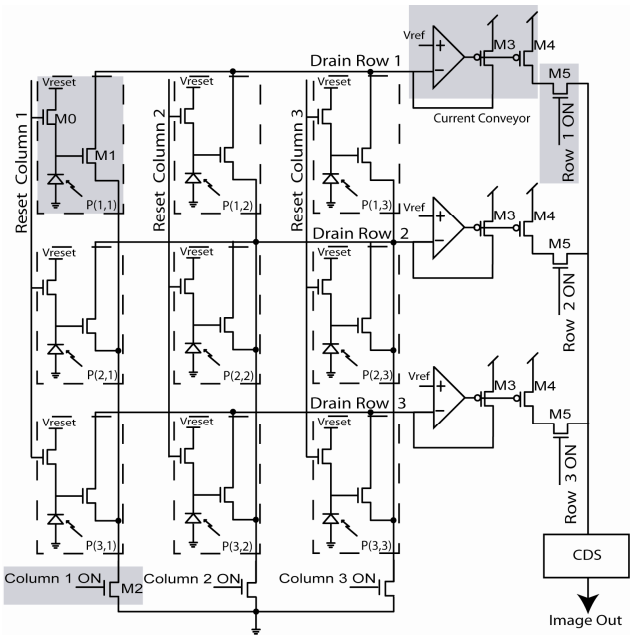


Figure 1: Pixel schematic and overview of the overall image sensor architecture

zero. In order to understand the control principle of the pixel, we should take a look at the circuitry which sets the drain and source voltage of the read out transistor M_1.

The voltage at the drain of transistor M_1 is determined by the reference voltage (V_{ref}) at the positive terminal of the operational amplifier and it is set to be ~0.2V. The operational amplifier is connected in a negative feedback via transistor M_3, effectively implementing a second generation current conveyor circuit. The output of the current conveyer is provided via transistor M_4, which replicates the input current provided form the photo pixel of interest. Both transistors M_3 and M_4 operate in saturation region, which ensures correct replication of the input photo current. The mismatches between transistors M_3 and M_4, which will cause gain error between columns, are minimized by using large aspect ratio transistors. The current conveyor effectively masks the parasitic capacitance on the drain line by pinning the input line to V_{ref}, leading to higher read out speed (or higher frame rates).

The drain voltage of M_1 transistor across all pixels, regardless whether they are in the on or off state, is always set to V_{ref}. Only the source voltage is manipulated in order to access a pixel. For example, if switch transistor M_2 in column 1 is turned on, the drain voltage of pixels numerated as P(x,1) for x=1 to N, where N is the number of pixels in the column (N=3 in Figure 1), are connected to ground. A V_{ds} drop of 0.2V is established across these transistors and their respective currents are provided in parallel on the horizontal busses to the column-parallel current conveyors.

When the switch transistor M_2 is turned off, the source voltage of transistor M_1 is floating and it will start to charge from 0 to 0.2V in order to turn off the pixel (V_{ds}=0). For a small imaging array, the time to charge up the source line can be faster then the minimum pixel scanning time and it will not cause problems during read out. For large imaging arrays and hence large parasitic capacitance, switch transistor M_2 should be implemented as a differential switch. This differential switch should temporarily connect the source of the transistors to 0.2V in order to speed up the charge up time and then the source line should be left floating. The source voltage should be left floating for the unselected columns because of the mismatching at the drain voltages due to offset error in the current conveyer i.e. operational amplifier. These voltage mismatches will cause various pixels during the off state to have a non-zero V_{ds} value and they will erroneously contribute to the final current output. If a non-floating differential switch should be implemented, amplifier offset compensation has to be implemented in order to compensate for mismatches in the column current conveyor voltage input.

Once a column is selected, all pixels within that column output their values to the respective column-parallel current conveyers. The next step is to select a particular row. This is achieved via the vertical switch transistor M_5. In Figure 1, the vertical switch transistors M_5 for row 1 is turned on, while switch transistor in rows 2 through K, where K is the number of columns, (K=3 in Figure 1) are turned off. Hence, only pixel P(1,1) is accessed and it is allowed to provide its output photocurrent to the correlated double sampling unit (CDS). Note that photo integration is performed per single row, since a single CDS unit and column parallel reset is employed.

At the end of the integration cycle, the photodiode voltage can be represented as V_{photo} and the integrated photo current is presented by equation 1.

$$I_{photo} = k_n \frac{W}{L}[(V_{photo} - V_t)V_{ref} - \frac{V_{ref}^2}{2}] \quad (1)$$

In equation (1), W/L is the aspect ratio, V_t is the threshold voltage and V_{ref} is the reference voltage across the drain and source terminal of M1 transistor. Once the integrated photo current is sampled on the current memory cell in the CDS unit, the pixel's photodiode voltage is set to V_{reset} by turning on M_0 transistor and a reset photocurrent presented by equation (2) is subtracted from I_{photo}.

$$I_{reset} = k_n \frac{W}{L}[(V_{reset} - V_t)V_{ref} - \frac{V_{ref}^2}{2}] \quad (2)$$

The final current output from the CDS unit is independent of the voltage threshold of M_1 transistor and it is presented by equation (3).

$$I_{out} = I_{photo} - I_{reset} = k_n \frac{W}{L} V_{ref}(V_{reset} - V_{photo}) \quad (3)$$

One of the main assumptions in the above equations is that the V_{ds} voltage across M_1 transistor remains constant during the integration and reset phase. This assumption is only valid in the case of ideal switch transistors, where the impedance is zero. If the switch transistor is embedded inside the pixel, due to space requirements, minimum size transistor is often used. Hence, the on resistance of the switch transistor can be considerable. For example, a minimum sized transistor in 0.5µ process, can have on resistance of ~2.5kΩ. If the difference in photo and reset current is ~10µA, the drain voltage of

transistor M_1 can vary ~25mV. Since typically two switch transistors are used for independent pixel access, these variations of the drain voltage can increase to 50mV. Variations along the drain line will degrade the linearity of the output and the precision of the CDS correction presented by equation 3.

In the proposed image sensor, the resistance due to switches along the direct path of the output photocurrent from transistor M_1 to the current conveyor is minimized. Only a single switch is used in this design together with a direct input to a column base current conveyor. Since the switch transistor M_2 is placed outside the imaging array, the aspect ratio can be made very large and the on resistance can be as small as ~12Ω. The input impedance of the current conveyer is ~10Ω and the drain voltage variations of M_1 are diminished down to 22μV. Since the on resistance of transistor M_2 is comparable to the input impedance of the current conveyer, two switch transistors outside the pixel and a global (chip-level) current conveyer can also be implemented. A global current conveyer would decrease the power consumption since only a single pixel would be connected to the output and it would alleviate column FPN problems. A global current conveyer would also demand individual pixel reset scheme and it will increase the number of reset transistors to two for a total of three transistors and an additional control line per pixel. Tradeoffs between speed, power and pixel size should be considered for an optimal implementation.

III. Image Sensor Measurements

The image sensor is composed of 50 by 128 pixels and is fabricated in a standard 1P3M CMOS 0.5 micron process. In Figure 2 the linearity of the output photocurrent from the pixel with respect to the integrated photodiode voltage, i.e. time, is measured. The pixel was reset at ~1.8msec for about 100 nsec. The reset current is 3.6μA and it can be manipulated by changing the reset voltage, V_{reset}, in Figure 1. When the reset transistor M_0 is turned off, charge injections at the photodiode node are observed. These charge injections have been minimized by using a minimum width reset transistor. Linear output photocurrent is observed during the integration phase. During the integration phase, the photodiode was discharged

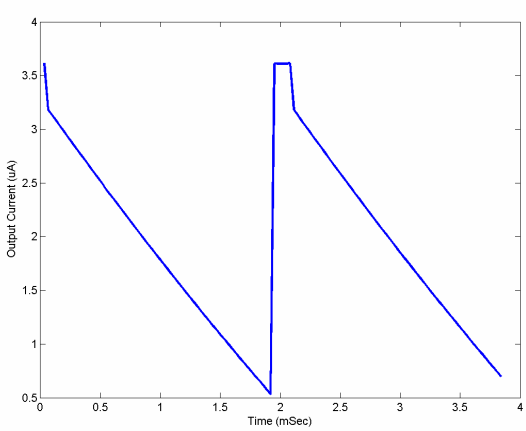
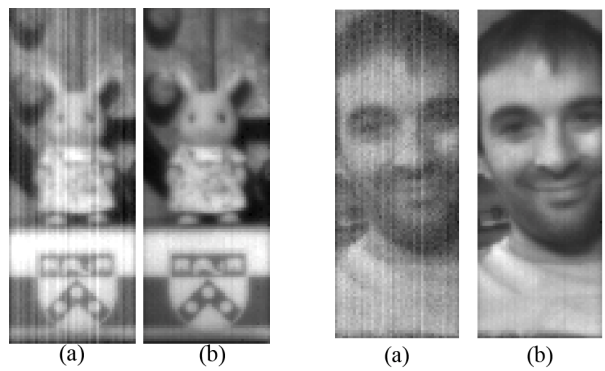


Figure 2: Measured linear current output with respect to photodiode integrated voltage.

by 1.1V, while >99.6% linearity was retained at the output photocurrent. The weak non-linearity can be due to the non linear discharge of the photodiode voltage or to mobility dependence on the gate voltage.

Figure 3 shows sample images recorded from the sensor. Images (a) in Figure 3 present the original image without any noise suppression. In these images, large variations across the entire image, as well as column variations are observed. Images (b) in Figure 3 present the result image after CDS noise suppression. In the noise corrected images, we can still observe column base FPN. This is due to the mismatches between transistor M3 and M4 in the column base current conveyer, which will induce column base gain errors in the output current. Column base (entire image) FPN on the corrected image is measured to be 0.35% (0.55%) of the saturated value. The uncorrected image has column base (entire image) FPN of 0.9% (1.5%) of the saturated value. The noise suppression unit has improved the spatial variations across the image by factor of 3. The low FPN figures are closely related to the improved linearity of the output photocurrent.



(a) (b) (a) (b)

Figure 3: Sample images from the sensor: (a) Uncorrected image and (b) Image after CDS noise cancellation.

IV. Temporal Noise Analysis of the 2T Pixel

Another important factor in evaluating the image sensor performance and limitations is temporal noise and the contributions of individual elements to the final temporal noise estimate. The effects on the decreased resistance of switch transistor M2 on the input referred noise and overall SNR are evaluated in this section.

The noise sources in a pixel can be divided into contributions from three different phases: shot and 1/f noise during the integration phase, thermal noise due to M_0 transistor during the reset phase and thermal noise due to M_1, M_2, current conveyer and CDS unit during the read out. The thermal noise contributions due to the current conveyer and the CDS unit are neglected in this analysis for simplicity reason. A simplified small signal model of the pixel is used to derive the input referred noise expression, where the current conveyer is substituted with an equivalent input resistance R_{CC} and a load capacitance C_0.

The reset noise and shot noise at the photodiode during the integration phase can be calculated via the well known equations presented in (4), where K is the Boltzmann constant, T is temperature, C_{photo} is the photodiode

capacitance and I_{photo} (I_{dark}) is the photo (dark) current at the photodiode.

$$\overline{V_{res}^2(t)} = \frac{kT}{C_{photo}} \text{ and } \overline{V_{int}^2(t)} = \frac{q(I_{photo} + I_{dark})T_{int}}{C_{photo}^2} \quad (4)$$

From the small signal model of the pixel circuit in Figure 1, we can derive the output referred noise due to M_1 and M_2 transistor. The output noise contributions at the current conveyor due to the read out transistor M_1 and switch transistor M_2 are presented by equation (5) and (6) respectively, where R_{CC} is the input impedance to the current conveyer, $R_{M1}(R_{M2})$ is the output impedance of transistor $M_1(M_2)$ and C_0 is the load capacitance at the current conveyer input.

$$\overline{I_{M1_Out}^2(t)} = \frac{kTR_{M1}}{C_0 R_{cc}(R_{M1} + R_{M2})(R_{M1} + R_{M2} + R_{CC})} \quad (5)$$

$$\overline{I_{M2_Out}^2(t)} = \frac{kTR_{M2}}{C_0 R_{cc}(R_{M1} + R_{M2})(R_{M1} + R_{M2} + R_{CC})} \quad (6)$$

In order to calculate the signal to noise ratio, equations (5) and (6) must be referred back to the input node i.e. to the gate of transistor M_1. The small signal circuit is used to determine the gain of the input (gate voltage of M_1) to the output of the circuit (current flowing through the current conveyor). The gain of the circuit is presented by equation (7), where G_m is the transconductance of transistor M_1. The SNR of the image sensor is then calculated by equation (8).

$$A = \frac{G_{M1} R_0}{R_{M1} + R_{M2} + R_{CC}} \quad (7)$$

$$SNR = 10 * \log \frac{(I_{photo} T_{int} / C_{photo})^2}{\overline{V_{res}^2(t)} + \overline{V_{int}^2(t)} + (\overline{I_{M1_out}^2(t)} + \overline{I_{M2_out}^2(t)}) / A^2} \quad (8)$$

The individual noise contributions and the total input referred noise are plotted as a function of the switch transistor impedance (R_{M2}) in Figure 4. The input referred noise due to the read out transistor M_1 as a function of R_{M2} is constant, while the input referred noise due to switch transistor M_2 as a function of R_{M2} monotonically increases. This is a result of dividing the output referred noise due to M_1 and M_2, which are proportional with $\sim R_{M2}^2$ and $\sim R_{M2}$ respectively, with the gain of the circuit, which is proportional with $\sim R_{M2}^2$. The overall signal to noise ratio has improved from 41.2dB for 10kΩ switch resistance to 43.3dB for 15Ω switch resistance (for estimated maximum non-saturated photocurrent of 360fA). Hence, the overall benefits by decreasing the switch resistance of M_2 are twofold. First, the linearity has been improved leading to lower spatial noise variations. Second, the overall SNR of the imager has been improved by ~2dB. The measured SNR of the image sensor is 42.5dB.

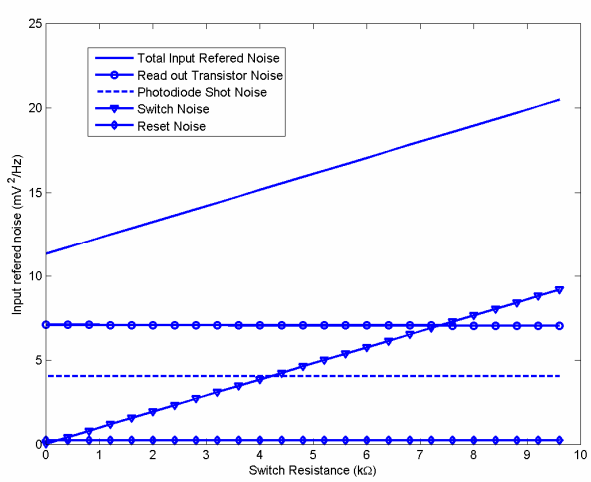


Figure 4: Input referred noise power due to photodiode shot noise, reset noise, switch and read out transistor as a function of the switch transistor impedance.

V. Summary

The 2 transistor image sensor is summarized in Table 1. The maximum scanning rate is limited by the virtual ground circuit to 50MHz. Using 50x128 (1000x1000) pixel array, a frame rate of 25k (41) frames per second can be achieved. The low fix pattern noise (0.35% of saturation current) is comparable to voltage mode APS. The low power consumption of this system of 5mW is another advantage of current mode imaging systems.

Technology	0.5 µm Nwell CMOS
No. Transistors	25K
Array Size	50 x 128
Pixel Size (Fill Factor)	10 µm x 10 µm (36%)
Chip Size	1.5mm x 3mm
FPN with CDS row (entire)	0.35% (0.55%)of sat. level
FPN without CDS row (entire)	0.9% (1.5%)of sat. level
Measured Input Referred Noise	7.5mV
SNR	42.5dB
Saturation level	3.5µA
Power Consumption	5mW

Table 1: Chips summary

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