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Abstract
High performance ambipolar silicon nanowire (SiNW) transistors were fabricated. SiNWs with uniform oxide sheath thicknesses of 6–7 nm were synthesized via a gas-flow-controlled thermal evaporation method. Field effect transistors (FETs) were fabricated using as-grown SiNWs. A two step annealing process was used to control contacts between SiNW and metal source and drain in order to enhance device performance. Initially ρ-channel devices exhibited ambipolar behavior after contact annealing at 400 °C. Significant increases in on/off ratio and channel mobility were also achieved by annealing.

Keywords
annealing, silicon, elemental semiconductors, nanowires, field effect transistors

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Systematic study of contact annealing: Ambipolar silicon nanowire transistor with improved performance

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High performance ambipolar silicon nanowire (SiNW) transistors were fabricated. SiNWs with uniform oxide sheath thicknesses of 6–7 nm were synthesized via a gas-flow-controlled thermal evaporation method. Field effect transistors (FETs) were fabricated using as-grown SiNWs. A two step annealing process was used to control contacts between SiNW and metal source and drain in order to enhance device performance. Initially *p*-channel devices exhibited ambipolar behavior after contact annealing at 400 °C. Significant increases in on/off ratio and channel mobility were also achieved by annealing. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2720309]

Silicon nanowires are among the most promising one-dimensional nanomaterials for future nanoelectronic devices.[1] Both *p* and *n* dopings of SiNWs can be achieved controllably, and SiNWs are compatible with existing high volume silicon manufacturing processes.[2] For future applications, the control of key field effect transistor (FET) parameters such as *p* or *n* type, threshold voltage, on/off ratio, and channel mobility is crucial. A conventional metal-oxide-semiconductor field effect transistor (MOSFET) utilizes heavily doped silicon as source and drain and operates in inversion mode whereby a gate bias is required to generate minority carriers.[3] However, most silicon nanowire field effects transistors (SiNW FETs) utilize metals as source and drain and operate in accumulation mode; a gate bias is required to generate majority carriers. It is well accepted that the characteristics of the latter are controlled by Schottky barriers between metal and conducting channels.[4,5] From our previous study, we ascribed relatively low on/off ratio and channel mobility to the existence of contact barriers.[6] Therefore, controlling metal/SiNW contacts is critical to achieve reliable high performance devices.

Silicide formation is one of the most effective ways to control and improve the contacts in bulk Si.[7] A two step annealing process is a very effective way to make reliable and low resistance nickel monosilicide (NiSi) in MOSFETs. Extensive studies focused on developing silicide formation for the 65 nm complementary metal-oxide-semiconductor (CMOS) technology node and beyond, and optimal processes to make self-aligned NiSi on top of a poly-Si gate were identified. The first annealing step between 250–350 °C forms Ni_2Si, while the second step between 400 and 450 °C is required to form low resistance NiSi in planar CMOS.[7] However, only a few rigorous studies have been done to investigate the effect of contact annealing on device performance and to find the optimized contact annealing processes in SiNW systems.[8]

Another challenge is to align individual *p*-type and *n*-type nanowires to make large-scale complementary logic circuits. Alternatively, an ambipolar FET is very attractive because it can work as either unipolar *p*-type or *n*-type FET by implementing different top gate metals and asymmetric design.[9] Extensive theoretical and experimental work has been done on complementary logic devices made of ambipolar carbon nanotube transistors,[9–11] while little is known about the fabrication of ambipolar FETs based on SiNWs.

We report the results of systematic annealing to control the properties of metal source and drain contacts to SiNW, and process optimization to achieve high performance ambipolar SiNW FETs.

SiNWs were synthesized via a thermal evaporation method without catalysts; details have been reported previously.[6] The original growth scheme was modified to attain better control of the growth conditions. We reversed the direction of gas flow during the slow ramping-up phase of the heating schedule to ensure that minimal Si flux arrived at the substrate before the pellet reached the desired temperature, 1230 °C. At this time the flow direction was reversed again to initiate growth on the collection wafer. After 30 min of growth the gas flow is again reversed to terminate growth at a known temperature as the furnace cools to ambient.

As-grown SiNWs were characterized using scanning electron microscopy (SEM) and transmission electron microscopy (TEM). SEM showed that most of the SiNWs were long, straight, and smooth, while TEM revealed crystalline cores covered with an amorphous oxide sheath. SiNWs grown using flow reversal had constant oxide sheath thickness of 6–7 nm regardless of the core diameter, whereas SiNWs in the previous work (without flow control) displayed a wide range of oxide sheath thicknesses of 4–12 nm.[12]

FETs were fabricated from SiNWs transferred onto degenerately boron-doped silicon substrates coated with 100 nm of stoichiometric silicon nitride (Si_3N_4). After locating the SiNWs with atomic force microscopy, source and drain were designed with 4 μm channel length. Electron beam lithography was used to define electrodes. The SiNW oxide sheaths in the contact regions were removed with buffered HF just before e-beam evaporation of the contacts. Two consecutive layers of 10 nm nichrome (NiCr, 80% Ni and 20% Cr) and 90 nm Au were deposited. NiCr was chosen as source and drain because Ni provides low contact resistance and excellent compatibility with nanoscale Si.[13] At the same

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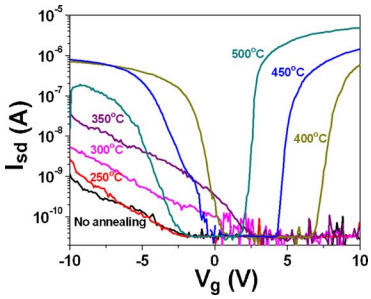

FIG. 1. (Color online) I-V_g characteristics of a SiNW FET (device A) recorded for $V_{sd}=+2$ V before and after contact annealing; no annealing and $T_2=250$, 300, 350, 400, 450, and 500 °C with fixed $T_1=200$ °C. The gate bias was swept from −10 to+10 V.

time, Cr reduces the thermal instability and poor adhesion of Ni.

Electrical transport measurements of SiNW FETs with no contact annealing were made at room temperature using the degenerately doped substrate as a back gate. After initial measurements, devices were placed in a vacuum furnace with a base pressure of 2×10^{-6} torr. A two step annealing process was used to form reliable contact between metal and SiNW. As the first step, SiNW FET was annealed for 2 min at 200 °C (T_1). As the second step, temperature was ramped up to $T_2=250$ °C and the sample was annealed for another 5 min. Electrical transport measurements were carried out immediately after these two steps. After this second set of measurements, further annealing at $T_1=200$ °C and at $T_2=300$ °C was performed and electrical transport properties again measured. This alternation between annealing and electrical measurements was continued on the same device with T_1 fixed at 200 °C and increasing T_2 in 50 °C increments up to 600 °C, above which significant degradation in electrical transport properties was observed. To rule out V_{th} shift from doping variations in different nanowires, we carried out contact annealing at different temperatures on the same device.

Figure 1 shows representative current versus gate voltage (I-V_g) characteristics of device A at fixed $V_{sd}=2$ V and for second annealing temperature T_2 from 250 to 500 °C. The gate sweep was from −10 to+10 V.[14] Devices with unannealed contacts always behave as p-channel enhancement mode (normally off) FETs; at $V_g=0$ V, current is only tens of picoamperes (instrument limited). The p-type behavior is attributed to accumulation of holes in a SiNW channel, while the normally off behavior at $V_g=0$ is attributed to carrier depletion caused by the Schottky barriers.[5] Enhancement mode is preferred for microprocessors and other logic devices due to faster operation and lower power consumption.[15] For the first few annealing cycles, current increases and threshold voltage (V_{th}) becomes more positive. At 400 °C a dramatic transition to ambipolar behavior is observed; now the I-V_g characteristic clearly shows accumulation with $V_g<0$, an insulating region, and an inversion region for $V_g>+7$ V. Such behavior requires both source and drain contacts with low barrier heights for majority and minority carriers, which can be switched between n channel and p channel. Therefore, the transition from unipolar p channel to ambipolar is attributed to significant improvement in contacts by annealing. Beyond 550 °C we observed performance degradation, possibly due to agglomeration of the contact metal films.

We also found that annealing first at 200 °C followed by 400 or 450 °C yielded ambipolar devices with improved performance parameters. The first step is crucial to limit Ni diffusion and to prevent excess silicide formation. It is also effective in removing moisture and organic solvents from lift-off, since the devices were not protected by a passivation layer such as polyimide or silicon nitride. Single step annealing at 450 °C for longer time converted the SiNW into a metallic nanowire. This underscores the importance of the two-step process for reliable SiNW contacts.

Table I summarizes the parameters of device A for different second-annealing temperatures T_2. Threshold voltage V_{th} is defined as the intersection of a straight line fitted to the linear region of $\log(I)$ vs V_g and $I=30$ pA. For ambipolar behavior, V_{th} for holes (h^+) represents the value of V_g at which hole conduction becomes dominant for a given V_{sd}; similarly for electrons (e^-) it represents the onset of dominant electron conduction. The hole conduction on/off ratio is a lower limit defined as the current at $V_g=-10$ V divided by the off current (I_{off}), the smallest measurable current in the off state; similarly for the electron conduction on/off ratio taken at $V_g=+10$ V. Effective channel mobilities (μ) were estimated using $dI/dV_g=\mu(C/L^2)/V_{sd}$, where dI/dV_g is the transconductance, μ is the carrier mobility, L is the length, and C is the capacitance. For this global back gate device geometry, the SiNW capacitance is given by $C\approx 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where r is the SiNW radius, ε is the gate dielectric constant, ε_0 is the permittivity of free space, and h is the gate dielectric thickness.[16] As well as the transition to ambipolar behavior, Table I clearly indicates significant improvement in both on/off ratio and mobilities by contact annealing.

To examine reproducibility of the annealing effects, we studied the properties of five more annealed devices (devices

TABLE I. Summary of the key parameters of a SiNW FET (device A) depending on second annealing temperatures T_2, each of which was preceded by a first anneal at $T_1=200$ °C.

Annealing temperature	No annealing	250 °C	300 °C	350 °C	400 °C	450 °C	500 °C
I ($V_g=-10$ V)	1.2 nA	2.6 nA	5.4 nA	41 nA	700 nA	790 nA	16 nA
I ($V_g=+10$ V)	28 pA	30 pA	52 pA	46 pA	600 nA	1.5 μA	4.8 μA
V_{th} for h^+	−1.8 V	−2.2 V	+3.0 V	+2.8 V	+0.3 V	0.0 V	−2.4 V
V_{th} for e^-	⋯	⋯	⋯	⋯	+6.9 V	+4.3 V	+2.0 V
On/off ratio (h^+)	40	84	190	1900	26 000	24 000	500
On/off ratio (e^-)	⋯	⋯	⋯	⋯	22 000	44 000	150 000
μ_h (cm^2/V s)	0.1	0.06	0.51	2.90	510	150	54
μ_e (cm^2/V s)	⋯	⋯	⋯	⋯	310	730	770

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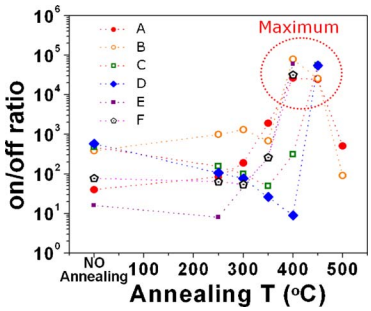

FIG. 2. (Color online) On/off ratios for hole conduction of six different devices (A–F) before and after contact annealing; no annealing and T_2=250, 300, 350, 400, 450, and 500 °C with fixed T_1=200 °C. Significant improvement in on/off ratio was achieved after annealing at T_2=400 and 450 °C.

B–F). Figure 2 shows on/off ratios for hole conduction of all six samples as a function of T_2. Consistent improvement in on/off ratio, peaking around 400–450 °C, clearly stands out from minor variations among the six samples. Contact annealing enhances the on/off ratio by two to four decades or more (limited by current noise in the experiment). Similarly, Fig. 3 shows hole and electron mobilities versus T_2. Empty circles and filled diamonds represent the effective hole and electron mobilities of each device, while the crosses are the average hole mobilities at each T_2. Significant increases were observed for both electrons and holes, and once again the enhancements were optimized at 400–450 °C, coinciding with the onset of ambipolar behavior. Improvement in channel mobilities up to four orders of magnitude was achieved by contact annealing. This ambipolar behavior is attributed to accumulation of holes with negative gate bias and to inversion of electrons with positive gate bias. Two step annealing formed metal silicides with very low resistance for hole and electron conductions. The optimal annealing conditions for SiNW are very similar to those for NiSi formation in CMOS technology.[7] It is very promising that the proven processes in CMOS are compatible with optimal processes for SiNWs. Further studies are required to explain the atom-scale mechanisms underlying the improved device performance and ambipolar transition.

Even though tremendous progress has been made to align *p*- and *n*-type SiNWs for logic devices, large scale complementary integrated circuits based on *p*- and *n*-type SiNWs face huge challenges.[1] In general, ambipolar behavior is not desired in CMOS because of the risk of high leakage current at the opposite polarity. However, an ambipolar FET can perform as unipolar *p*-type or *n*-type device by engineering the top gate geometry and materials. For example, metals having different work functions can shift the threshold voltages in either direction.[17,18] Therefore, large scale alternating *p*- and *n*-type NW FETs can be made by alternating the gate metal on a very long SiNW. Recently, scientists at IBM demonstrated the first large scale logic device using ambipolar carbon nanotube FETs. They used Pd for *p*-type FET and Al for *n*-type FET.[9] The results presented here suggest that SiNW device development will benefit directly from extensive current efforts to find the best gate metals for bulk *p*- and *n*-channel MOSFETs.[19,20]

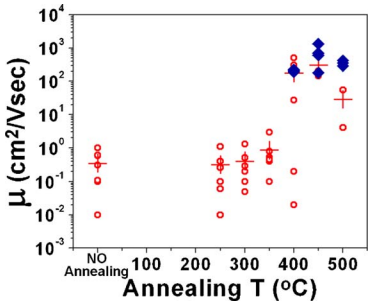

FIG. 3. (Color online) Channel mobilities for hole and electron of six different devices (A–F) before and after contact annealing; no annealing and T_2=250, 300, 350, 400, 450, and 500 °C with fixed T_1=200 °C. Significant improvement of mobilities and onset of ambipolar transition was achieved after annealing at T_2=400 and 450 °C.

In conclusion, we achieved high performance ambipolar SiNW FETs using a two step contact annealing. Single crystalline SiNWs with uniform oxide sheath were prepared by a gas-flow-controlled thermal evaporation method. Electrical transport measurements performed on both as-prepared FETs and contact annealed FETs. An as-prepared SiNW FET behaved as a *p*-channel enhancement mode FET. After contact annealing, dramatic transition to an ambipolar FET was achieved. Ambipolar SiNW FET is one of the most promising candidates for future nanoelectronic applications. Understanding of different device physics and fabrication methods in SiNW is crucial to extend further scaling for the next generation.

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