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Synthesis and Post-growth Doping of Silicon Nanowires

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ABSTRACT

High quality silicon nanowires (SiNWs) were synthesized via a thermal evaporation method without the use of catalysts. Scanning electron microscopy and transmission electron microscopy showed that SiNWs were long and straight crystalline silicon with an oxide sheath. Field effect transistors (FETs) were fabricated to investigate the electrical transport properties. Devices on as-grown material were p-channel with channel mobilities 1 - 10 $cm^2 V^{-1} s^{-1}$. Post-growth vapor doping with bismuth converted these to n-channel behavior.

One-dimensional nanostructures such as semiconductor nanowires (NWs) and single walled carbon nanotubes (SWNTs) are attractive components for future nanoelectronic applications since their structure, size and electronic properties are suitable for nanoscale devices.[1,2,3] Nanowires of silicon are of primary interest due to their compatibility with existing process technology in IC industry.[4] Several synthesis routes are available, the most popular being chemical vapor deposition (CVD), pulsed laser vaporization (PLV) and thermal evaporation (TE).[5,6,7,8] Field effect transistors (FETs), biosensors, diodes and logic gates were realized using silicon nanowires (SiNWs) synthesized by CVD.[9,10] Both CVD and vapor-liquid-solid (VLS) PLV require catalysts, while oxide-assisted thermal evaporation is catalyst-free. This is potentially a major advantage in terms of purity control, especially trace metals. Little is known about the transport properties and device characteristics of thermal evaporation SiNWs, on which we focus in this report. In addition, it is important to control dopant type and concentration if SiNWs are to be reliable materials for nanoscale electronic devices. Given the small length scales compared to bulk or thin films, new doping concepts need to be devised. Remarkable progress in n type and p type doping during synthesis of SiNWs via CVD has been made, by adding vapor precursors containing boron or phosphorus to SiH_4.[11] To the best of our knowledge, post-growth doping of SiNW has not been attempted heretofore. Here, we studied the electrical transport properties of both FETs of as-synthesized SiNWs and post-growth doped SiNWs.

SiNWs were synthesized via a thermal evaporation method without the use of catalysts. A wafer of degenerately boron doped silicon was crushed with pestle and mortar, and 0.2 g of the resulting powder was pressed into a pellet. The pellet was placed near the center (hot zone) of an alumina tube, while a bare silicon substrate was placed near to the downstream end of the tube. The tube was then loaded into a horizontal flow furnace, so as to place the pellet at the hot zone. A mixture of 10% hydrogen in helium was piped through a cold trap immersed in liquid nitrogen, and flowed through the furnace at a rate of

50 sccm. The nitrogen trap maintained the H_2O/H_2 ratio below the critical value for SiO_x reducing conditions.[12] After a brief purging period, the temperature at the hot zone was ramped up to 1230 °C and held there for 500 min. During this period, SiNWs grew on the substrate, which was maintained at temperatures of 1000 °C. At the end, the furnace was allowed to cool to room temperature.

The substrate was retrieved from the furnace and examined as-is with a scanning electron microscope (SEM). Dense mats of long and straight nanowires, with diameters ranging between 10-40 nm were obtained. Most of these wires were many tens of micrometers long and intermixed with many bunches of necklace-like nanostructures with a "string of pearls" morphology. Transmission electron microscope (TEM) samples were prepared by gently pressing a holey carbon coated TEM grid onto the growth substrate. A JEOL 2010F, equipped with a Gatan Imaging Filter (GIF) for electron energy loss spectroscopy (EELS) and an x-ray energy dispersive spectroscopy (XEDS) analyzer, was operated at 197 kV for the characterization work. These confirmed that the material contained only silicon and oxygen. It is not a trivial task to distinguish the crystalline and non-crystalline phases by conventional TEM imaging. Energy filtered TEM (EFTEM) was thus employed to perform chemical mapping so as to distinguish crystalline Si from amorphous SiO_2. Exploiting the well known difference in the peak plasmon loss between Si (~17 eV) and amorphous SiO_2 (~23 eV), a series of EFTEM images were acquired at 1 eV intervals between 10-30 eV.[13] The stack of EFTEM images was used to construct the color-coded map of the chemical environment of Si shown in figure 1(a). In this map, red represents crystalline Si, and green represents amorphous SiO_2. The chemical map unequivocally shows that the straight nanowires have a crystalline Si core sheathed with amorphous SiO_2, while the necklace-like structures are crystalline Si "pearls" connected by amorphous SiO_2 "strings". This particular image shows a helical nanowire of amorphous SiO_2, but this kind of nanostructure is comparatively rare.

In agreement with the results from the chemical map, only nanostructures with crystalline cores produced diamond cubic Si diffraction patterns in selected area (SAED) and convergent beam electron diffraction (CBED) studies. In addition, high resolution TEM images showed the presence of lattice defects in many SiNWs. For example, stacking faults in <111> grown SiNW, indicated by the black arrow, can be seen in figure 1(b). Inset is the associated CBED pattern from the SiNW. We have observed the common growth directions of <111> and <112> in our SiNWs. We measured the diameters of the crystalline cores from a large number of nanowires from TEM images and found a range of core diameters between 5-20 nm and oxide thicknesses between 4-12 nm.

FETs were fabricated from SiNWs transferred onto degenerately doped silicon substrates covered with 100 nm of stoichiometric silicon nitride (Si_3N_4). The as-grown SiNWs were transferred from the initial growth substrate to the new FET substrates by gently pressing the substrates together. After locating the SiNWs with atomic force microscopy (AFM), source and drain structures of FETs were defined by electron beam lithography (EBL). The SiNW oxide sheaths in the contact regions were removed with buffered oxide etchant (BOE) just before thermal evaporation of Ti/Au contacts.

Electrical transport measurements of SiNW FETs were made at room temperature, operating the degenerately doped silicon substrate as a global back gate. Figure 2 shows representative current vs gate voltage ($I\text{-}V_g$) characteristics of a SiNW FET at a fixed $V_{sd} = 0.2$ V, while the inset shows a set of current vs source drain voltage ($I\text{-}V_{sd}$) characteristics at different gate voltages. The measured $I\text{-}V_g$ response is characteristic of a p-channel FET with a sharp turn on/off behavior and with hysteresis depending on two different gate sweep directions. This hysteresis behavior is attributed to injection of charges into traps in the gate dielectric layer. The injected charges generate additional electric field to gate bias and change the threshold voltage of gate response. Details of this mechanism were previously studied in carbon nanotube based FET devices and widely accepted.[14] Although we are unable to provide evidence for the presence of boron due to detection difficulties, we believe that boron in the source pellet was incorporated into the synthesized SiNWs, rendering them p-type.

Channel mobilities were estimated using $dI/dV_g = \mu(C/L^2)/V_{sd}$, where dI/dV_g is the transconductance, μ is the carrier mobility, L is the length and C is the capacitance. For this global back gate device geometry, the SiNW capacitance is given by $C \approx 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where r is the SiNW radius, ε is the gate dielectric constant, ε_0 is the permittivity of free space and h is the gate dielectric

thickness.[15] From the slope of linear region of the I-V_g curve, the transconductance was 12 nS, yielding a carrier mobility of about 6.8 cm^2 V^{-1} s^{-1}. It is a lower bound due to possible existence of barriers between metal contacts and nanowire. The mobility values of 12 FETs from our synthesis range between 1 and 10 cm^2 V^{-1} s^{-1}. Our values are very close to the 10-100 cm^2 V^{-1} s^{-1} carrier mobilities observed in bulk p-channel Si MOSFETs with 10 nm channel width, although it is still far lower than the hole mobility in intrinsic bulk silicon (450 cm^2 V^{-1} s^{-1}).[16,17] For comparison, the same calculation yielded ~ 50 cm^2 V^{-1} s^{-1} for a CVD SiNW from published data.[18]

To fabricate n-type SiNWs, vapor phase doping of SiNWs was performed using bismuth vapor in evacuated quartz tubes. Bismuth has relatively high vapor pressure, and is a frequently used donor in bulk silicon.[19] Bismuth powder was placed near the closed end of a quartz tube. As-grown SiNWs were transferred onto a new substrate and the substrate was placed in the quartz tube a few inches away from the Bi powder. The quartz tube was then pumped down to a vacuum of 10^{-6}–10^{-7} torr with a turbomolecular pump, and sealed under dynamic vacuum. The sealed quartz tube was annealed in a furnace at 1000 °C for 1 hour to vaporize the Bi source and to achieve dopant diffusion into the SiNWs. After the diffusion anneal, the substrate was recovered from the quartz tubes and spin-coated with PMMA resist. Electrode patterns were written with EBL and Ti/Au contacts were deposited by thermal evaporation.

The electrical characteristics of the SiNW FETs fabricated from the Bi-doped material show that vapor phase Bi-doping can effectively dope the as-grown p-type material into n-type SiNWs. Figure 3 shows a representative I-V_g characteristic at a fixed V_{sd} = 2 V, while the inset shows a set of I-V_{sd} characteristics at different gate voltages. The gate dependence of the I-V_{sd} curves shows that the Bi-doped SiNWs are n-type. However, we found that the doping level varied significantly from SiNW to SiNW. While most FETs (7 out of 9) showed n-channel behavior, two FETs showed 10 times higher zero gate conductance and no turn-off in the gate voltage range of ±5 V.[20] These latter devices behave like degenerately doped metallic NWs. We believe that the variation in doping concentration is due to the variable oxide thickness which limits dopant diffusion into SiNWs. As mentioned before, our growth process yielded oxide sheaths with variable oxide thickness ranging from 4 to 12 nm, substantially thicker than typical 1-2 nm native oxide from CVD NWs. SiNWs with thick (thin) oxide sheaths present greater (lesser) barrier to Bi diffusion into Si core and are consequently lightly (heavily) doped.

In conclusion, single crystalline silicon nanowires (SiNWs) sheathed with oxide were prepared by thermal evaporation without the use of catalysts. Electrical transport measurements were performed at room temperature. FETs made of as-grown SiNWs from p-type source materials behave as p-channel devices. Using bismuth vapor, the as-grown SiNWs were doped into n-type materials with various doping concentrations depending on the oxide sheath thickness. The majority carriers in SiNWs can therefore be compensated by appropriate choice of the vapor phase dopant species. We anticipate that more sophisticated devices such as diodes or bipolar transistors can be obtained using our post-growth doping technique by selective patterning and doping of the SiNWs.

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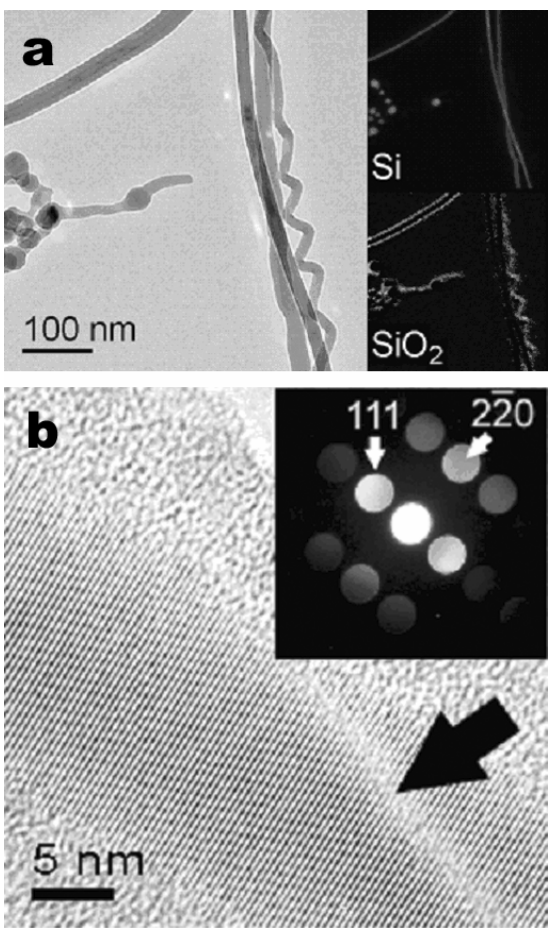

FIG. 1. (Color online) (a) EFTEM images were used to construct a color-coded map of the chemical environment of Si, where red represents crystalline Si, and green represents amorphous SiO_2. (b) A high resolution TEM image of a SiNW grown along <111>. The black arrow indicates the location of a stacking fault in the SiNW. Inset is the associated CBED pattern of the SiNW, taken along $\langle 11\bar{2} \rangle$. The (111) and $(2\bar{2}0)$ disks are labeled.

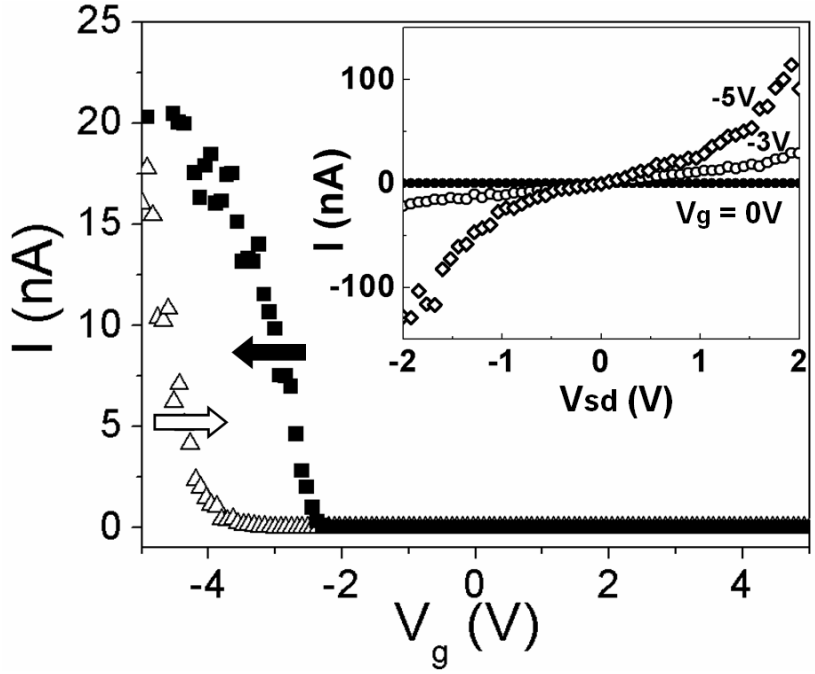

FIG. 2. I-V_g data of an as-grown SiNW FET recorded for V_{sd} = 0.2 V. The threshold voltages of the device depend on the gate sweep directions. Empty triangles represent the gate bias sweep from -5V to +5V while filled squares represent the gate bias sweep from +5V to -5V. (inset) a set of I-V_{sd} data recorded at different gate voltages.

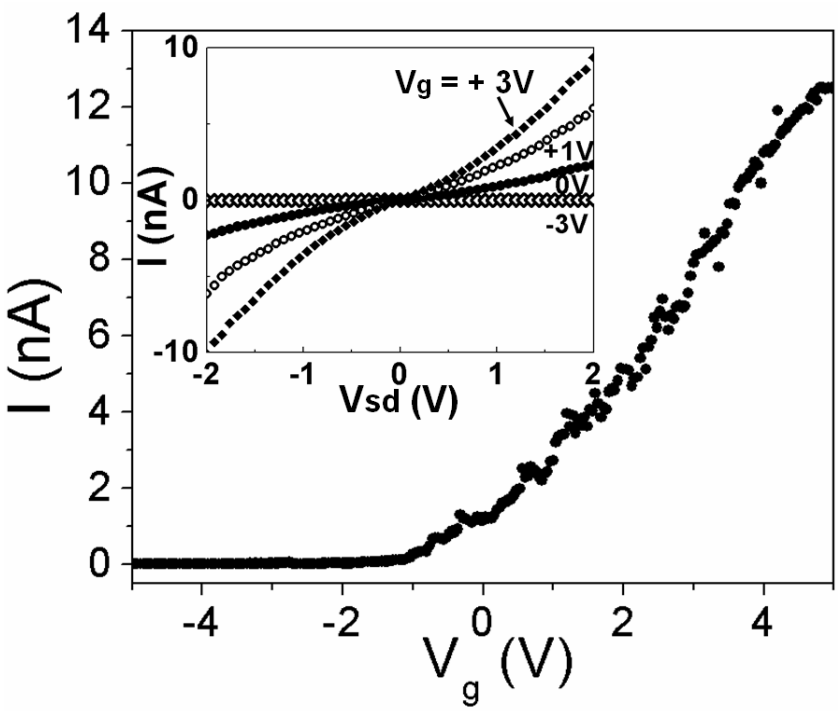

FIG. 3. I-V_g characteristic of a Bi-doped SiNW FET recorded for V_{sd} = 2 V. (inset) a set of I-V_{sd} data recorded at different gate voltages.