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Abstract
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SILICON NANOWIRES: DOPING DEPENDENT N- AND P- CHANNEL FET BEHAVIOR

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ABSTRACT

The electrical transport properties of field effect transistor (FET) devices made of silicon nanowires (SiNWs) synthesized by pulsed laser vaporization (PLV) were studied. From as-grown PLV-SiNW FET, we found p-channel FET behavior with low conductance. To improve conductance, spin on glass (SOG) and vapor doping were used to dope phosphorus and indium into SiNW, respectively. From doping after synthesis, we could successfully make both n- and p-channel FET devices.

INTRODUCTION

One-dimensional nanostructures such as SiNWs are promising materials for nano-scale electronic devices because they are considered as alternatives to conventional lithography-based devices [1]. Moreover, the electrical and optoelectronic properties of SiNWs can be tailored by dopant concentration and by quantum confinement for diameters of order 5nm or less [2].

Transport properties, namely conductance and mobility, are essential parameters to control in device fabrication. Those properties can be measured from current-voltage characteristics and gate dependence of SiNW-FET. Moreover, it is important to control dopant type and concentration so that SiNW will be reliable building blocks for nanoscale electronic devices. Since SiNW is a totally different system from bulk or thin film silicon, new concepts of doping need to be devised. So far, there has been remarkable progress in n and p doping during synthesis [3]. While this is simple and efficient using CVD, post-synthesis doping can provide additional flexibility in device design, doping control and selectivity for more sophisticated device structures. In this study, we report two new ways to achieve chemical doping after synthesis, customized for application to SiNWs.

EXPERIMENTAL DETAILS

SiNW-FET devices were fabricated using SiNWs from PLV growth process. Silicon target containing 10 at% iron catalyst was heated to $1100^{o}C$ in flowing argon and vaporized using a pulsed laser. The details are given elsewhere [4]. Previous TEM and AFM studies showed that these wires have silicon crystalline core diameter of 6.7 ± 2.9 nm surrounded by an amorphous SiO_x sheath of 1-2nm [4].

Doping SiNW was done by spin on glass (SOG) or vapor phase doping method after SiNW synthesis. To make n-type SiNW, conventional SOG is modified to dope phosphorus into SiNW [5]. Modification of doping conditions is necessary because the high temperature diffusion process with oxygen ambient designed for silicon wafer will result in total oxidation of very thin SiNWs. Therefore, phosphorus containing glass was deposited on SiNW previously deposited on silicon chips, and then the sample was placed in preheated furnace at 950℃ for 30 minutes with argon flow rather than the usual mixture of oxygen and nitrogen.

To fabricate p-type SiNW, vapor doping using indium in evacuated quartz tubes was performed. Indium has relatively low melting point and high vapor pressure, and is a frequently used acceptor in bulk silicon [6]. Indium powder was placed near the closed end of a quartz tube. Si wafer with SiNWs was located a few inches away from the powder. Turbo-molecular pump was used to achieve 10^{-6} to 10^{-7} torr vacuum. After sealing under dynamic vacuum, the quartz tube was moved to the furnace. Silicon wafer with SiNW was located where the temperature (doping temperature) is high enough to diffuse indium into silicon.

One challenge in diffusion doping SiNWs is that high temperature is incompatible with thin film metal alignment markers. To overcome this, we used random e-beam lithography patterning after doping. Ti/Au electrodes were deposited using thermal evaporation.

RESULTS AND DISCUSSION

From two probe measurements on as-grown PLV-SiNW, Ti electrodes were found to have the lowest contact resistance compared to Cr, Al and Au-Pd. The apparent 2-probe resistivity is the sum of contact and intrinsic NW resistances. Therefore, the identification of the resistance from wire itself requires four probe measurement. We used an electrometer with > 100 TΩ input impedance to measure the voltage drop across the inner electrodes 2 and 3 (V_{23}). Current flowing though 1 to 4 (I_{14}) is measured by a picoammeter. Since negligible current flows through the electrometer, V_{23} is the correct potential drop in the nanowire. Assuming that wire diameter is uniform and that resistance is linear with length,

$$R_{14}(\text{calculated}) = R_{23} \cdot \frac{L_{14}}{L_{23}}$$

$$R_c = R_{14}(\text{measured}) - R_{14}(\text{calculated})$$

Figure.1 is the result of four probe measurement vs. bias voltage. As shown, the contract resistance is about 1GΩ and at most, about 20% of total measured resistance. Therefore, we conclude that high resistance is an intrinsic property of these SiNWs. The actual resistivity of silicon nanowire is about 100 Ωcm, which for bulk Si would correspond to a doping concentration in the range 10^{13} to 10^{14} /cm^3. It is unlikely that the level of chemical purity implied by this range is actually achieved in the synthesis process. Thus we look for an alternative explanation of the high resistivity.

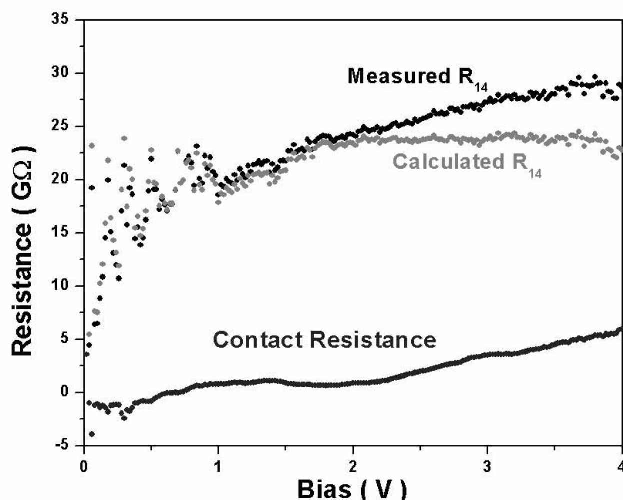

Figure 1. Four-probe resistance measurement of as-grown PLV-SiNW. Contact resistance is the difference of calculated resistance from measured resistance between outer electrodes.

The gate characteristics of undoped silicon nanowires were used to identify the majority carrier type and channel mobility. Figure 2 shows a gate sweep of as-grown SiNW-FET. With negative gate voltage, drain current increases rapidly while positive gate voltage suppresses the drain current dramatically. It is typical p-channel behavior with hysteresis depending on two different gate sweep directions. This hysteresis behavior is attributed to injection of charges into traps in silicon oxide layer. The injected charges generate additional electric field to gate bias and change the threshold voltage of gate response. Details of this mechanism were previously studied in carbon nanotube based FET devices and widely accepted [7]. The channel mobility of holes was obtained from transconductance(dI/dV_g) as 0.16cm^2/Vsec. For comparison, the hole mobility in intrinsic bulk silicon and 10nm CMOS channel mobility is 450 and 10-100cm^2/Vsec, respectively, much greater than observed here [8, 9]. The hole mobility in PLV-SiNWs is

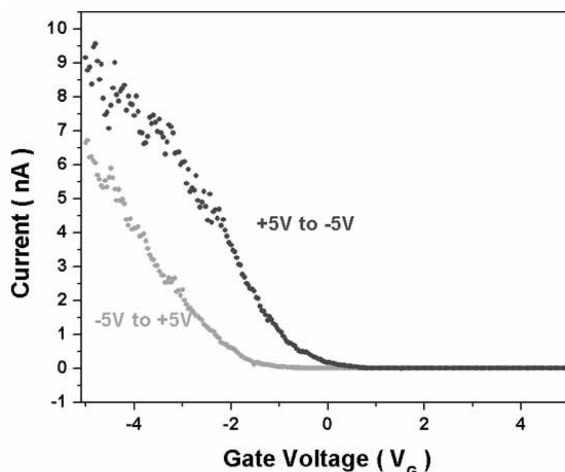

Figure 2. Gate dependence of PLV-SiNW FET showing p-channel behavior despite absence of intentional doping.

reduced significantly. We attribute low mobility of PLV SiNW to electrically active defects and/or excess scattering at the nanowire/oxide interface [10]. One possible source of excess defects is the few hours sonication used to produce SiNW in suspension.

For future application in diodes or transistors, it will be crucial to dope silicon nanowires to tailor their electrical properties. Few studies of SiNW doping have been carried out so far. Highly doped p-type and n-type wires respectively are obtained by the addition of B_2H_6 or red phosphorus to SiH_4 gas during CVD synthesis [3]. To the best of our knowledge, doping of SiNWs after synthesis has not been investigated to date. In principle, post-doping schemes should provide better control of concentration and afford the option of spatial selectivity.

Conventional SOG, based on sol-gel chemistry, is a standard IC industry process for phosphorus n-doping. As noted above, some modifications were required to adapt this method for nanowires. Figure 3 shows I-V curves taken as a function of gate voltage, indicating the conversion from p- to n-channel behavior. However, the 2-probe resistivity is 130 Ωcm, much higher than we expected. Evidently the diffusion of P into the wire was barely sufficient to compensate the initial p-channel behavior. The data in Figure 3 suggest very low mobility for this low carrier density n-channel device.

P-type doping was conducted using indium, which has a low melting point but relatively high saturation vapor pressure. It is also a common p-type dopant in bulk Si. This method again relies on diffusion into the wire, so we chose doping temperatures based on previous studies of In diffusion into bulk Si [6], namely 900, 1000 and 1100°C for one hour in evacuated quartz tubes. After doping, electrode patterns were randomly written using e-beam lithography and Ti/Au electrodes were deposited using thermal evaporation.

Figure 4(a) shows I-V characteristics for different doping temperatures, and Figure 4(b) shows the dependence on doping temperature of the 2-probe resistance. The resistance in the undoped state was about 30GΩ. After doping, resistance decreased significantly to 560 KΩ, 1.37 MΩ and 250 MΩ for 1100°C, 1000°C and 900°C indium doping, respectively.

The gate response of indium doped SiNWs is shown in figure 5. Doping temperatures of 1000 °C or greater yield devices which cannot be turned off for the range $-1.5\ V < V_g < +1.5\ V$. This behavior could be due to very high doping concentration, close to degenerate. More

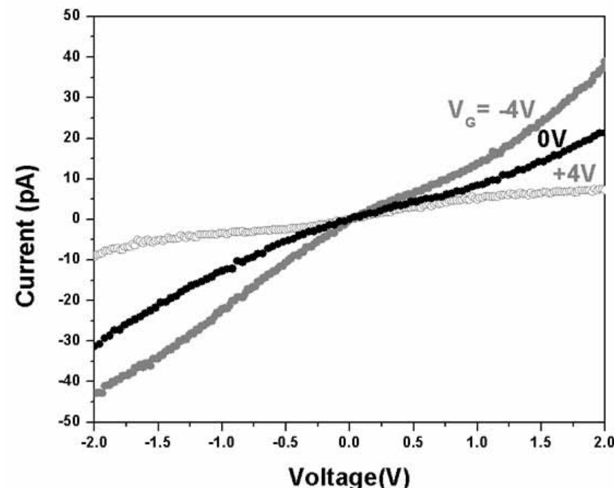

Figure 3. Gate dependence of phosphorus doped SiNW FET, suggestive of n-channel behavior with low mobility. Undoped wires give p-channel behavior, Fig. 2.

encouraging is the device doped at 900°C which showed p-channel behavior with low turn-on voltage. The channel mobility from transconductance is about 0.2cm^2/Vsec, similar to that of the undoped device. The results from overall devices are summarized in Table I.

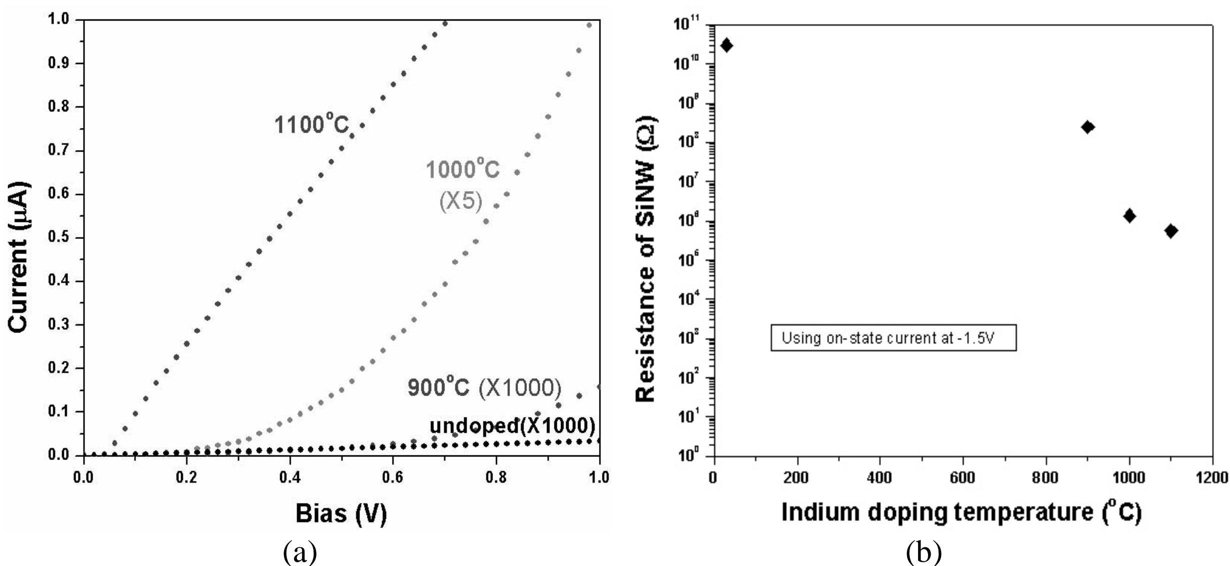

Figure 4. (a) I-V of p-channel FET device made of SiNW doped with indium at different temperatures. (b) R vs. doping temperature (semi-log scale)

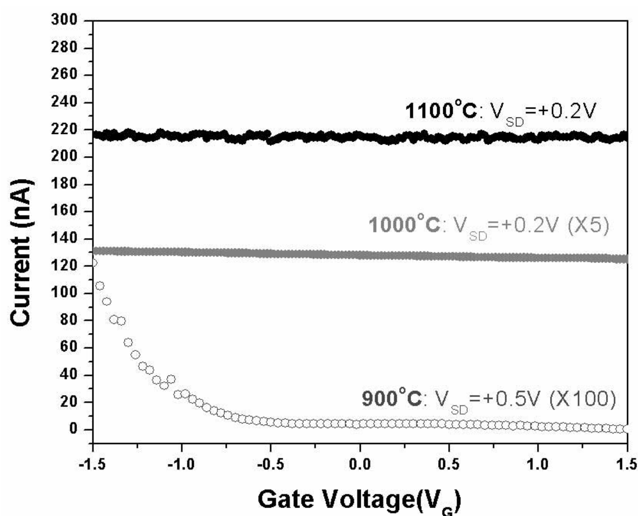

Figure 5. Gate dependence of indium doped SiNW-FET. Doping was conducted at various temperatures.

Table Ⅰ. Summary of undoped, phosphorus doped and indium doped PLV-SiNW FET devices

	Undoped SiNW	Phosphorus doped SiNW	Indium doped SiNW
Gate response	p-type	n-type	p-type
Resistivity	100 Ωcm	130 Ωcm	0.01 to 5 Ωcm
mobility	0.16 cm^2/Vsec	very small	0.20 cm^2/Vsec

CONCLUSIONS

The electrical properties of PLV-SiNW were studied. SiNW-FET device made of PLV-SiNW had high resistivity and low mobility compared to previously reported SiNW-FET based on CVD-SiNW. To modify conductivity and majority carrier type, phosphorus-doped spin-on glass and indium vapor were tested. I-V and gate response were compared before and after doping. With P-glass we found that the FET behavior changed from p- to n-type. With indium vapor doping, we found that the resistivity of FET depends strongly on the doping temperature, ranging from degenerately doped to p-channel behavior. From this study, we developed simple but reliable way to realize both n- and p- channel FET devices based on PLV-SiNW by doping after synthesis.

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REFERENCES

1. Y. Cui and C. M. Lieber, Science **291**, 851 (2001)
2. D. V. Melnikof and J. R. Chelikowsky, *Phys. Rev. Lett.* **92**(4), 046802 (2002).
3. Y. Cui, X Duan, J. Hu and C. M. Lieber, *J. Phys. Chem. B.* **104**(22) 5213 (2000).
4. R. J. Barsotti, J. E. Fischer, C. Lee, J. Mahmood, C. K. W. Adu, P. C. Eklund, *Appl. Phys. Lett.* **81**(15), 2866 (2002)
5. B. Hartiti, A. Slaoui and J. C. Muller, *J. App. Phys.* **71**(11) 5474 (1992)
6. S. V. Kolluri and A. N. Chandorkar, *J. Vac. Sci. Tech. A.* **11**(5) 2849 (1993)
7. M. Radosavlievic, M. Freitag, K. V. Thadani, and A. T. Johnson, *Nano Lett*. **2**(7) 761 (2002)
8. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, New York, 1981) p. 851
9. S. Takagi, A. Toriumi, M. Iwase, and H. Tango, *IEEE Trans Elec Dev.* **41**(12) 2357 (1994)
10. A. Baumer, M. Stutzmann, M. S. Brandt, F. C. K. Au and S. T. Lee, *Appl. Phys. Lett.* **85**(6), 943 (2004)