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ANALYSIS OF CLOCK BUFFER PHASE NOISE

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ABSTRACT

This paper presents a phase noise model for clock buffers. The model can be used to predict the phase noise introduced by clock buffers and to gain insight into phase noise transfer mechanisms in clock buffers. Based on the models, techniques for low phase noise clock buffer design are derived. The analytical results presented here have good agreement with simulation and measurement results.

1. INTRODUCTION

Clock buffers are widely used in microprocessors and other synchronous communication chips in which a global clock signal is distributed throughout the chip. In addition to that, ring oscillators that are used in phased-locked loops (PLL) for clock and data recovery, frequency synthesis, and clock synchronization consist of clock buffers, used as delay cells. The noise produced in these clock buffers adds random perturbations to the phase of the clock. These perturbations set a limit on the sensitivity of systems, such as receivers, detectors, and data transmission links whose performance relies on the precise periodicity of the clock.

A considerable amount of research has been done on the phase noise of practical oscillators [1][2][3]. However, these models are applicable to oscillators. Noise from clock buffers, which are components of ring oscillators, has not been considered. Clock buffers add jitter or phase noise to the clock signal at every instance where they are deployed in the clock distribution network. Low phase noise clock buffer design is very important to high-speed chip design. This paper establishes a noise model for clock buffers. This noise model is not only valuable in for the design of low phase noise clock buffers, but can aid in the design of low noise ring oscillator, which are configured in a positive feedback loop of clock buffers (i.e., delay cells).

The paper is organized as follows. Clock buffer noise model is presented in section 2. In section 3, the design implications of clock buffers to be derived from this model are described. Section 4 provides the simulations and experimental results that illustrate the accuracy of this model. Finally the conclusions are given in section 5.

2. CLOCK BUFFER NOISE MODEL

A typical clock buffer is shown in Figure 1. Suppose a clean clock is applied to the input of the cell, the output clock will have jitter or phase noise associated with it. The sources of this jitter include device thermal noise, flicker noise, and power supply rail noise within the buffer.

If we treat each of noise sources as inputs and the phase noise of the output clock as the output, a clock buffer can be modeled as a multiple-input and single-output (MISO) system. Each input is associated with one noise source in the buffer. For each input source, as explained in [3], a clock buffer can be modeled as a linear, timing-variant (LTV) system. The LTV system can be characterized by the impulse response function as shown in Figure 2. Noise input is in the form of current source, $i_{noise}(t)$, injected into the clock buffer. The resulting output phase noise is $\phi(t)$. A clock buffer is a memoryless system. An impulse input source will result in a similar phase noise impulse at the output shifted in time (Let us assume zero shift time here without losing any generality). The phase noise of the system is time dependent. That is to say, the output phase noise is dependent upon where noise is injected in the system. For example, if noise current is injected at a zero crossing point, it will cause a maximum phase shift in the output waveform because any voltage drifting will result the timing changes, i.e. the slope of the curve or the magnitude of transfer function is a maximum at the crossing point. If the noise current is injected at the peak of the signal, there is no phase noise for the output because any voltage change will only cause the magnitude of the output clock change without affecting the timing information, i.e. transfer function is at the minimum at the peak of the signal [3]. Therefore, impulse response function is a function of time t and the instant τ when the noise current is injected. The impulse response can be written as (1):

$$h_{\phi}(t, \tau) = \frac{\Psi(\tau)}{q_{max}} \delta(t - \tau) \quad (1)$$

where q_{max} is the maximum charge displacement on the noise injection node and $\Psi(t)$ indicates the amount of

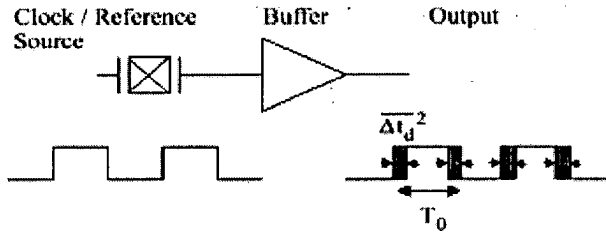


Figure 1. A Typical Clock Buffer

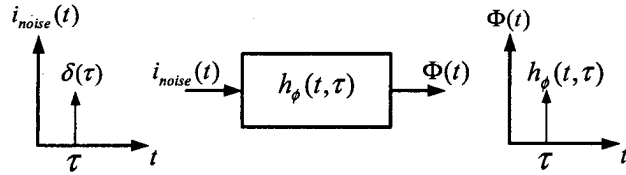


Figure 2. The Impulse Response of the Clock Buffer LTV System

phase shift resulting from applying a unit impulse current at time t on this node, δ is the delta function as defined in (2).

$$\delta(t) = \begin{cases} 1 & t = 0 \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

Because the input is a periodic clock signal, $\Psi(t)$ is also a periodic signal with the same period as the input clock. The typical $\Psi(t)$ is shown in the Figure 3.

Since $\Psi(t)$ is a periodic signal, it can be expanded into a Fourier series as (3).

$$\Psi(t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \quad (3)$$

where

$$c_0 = \frac{2}{T} \int_0^T \Psi(t) dt$$

$$c_i = \frac{2}{T} \int_0^T \Psi(t) \cos(n\omega_0 t + \theta_n) dt \quad (i = 1, 2, \dots, \infty) \quad (4)$$

When the noise current $i_{noise}(t)$ is injected, the output phase noise can be found from the following convolution (5).

$$\phi(t) = \int_{-\infty}^{+\infty} h_{\phi}(t, \tau) i_{noise}(\tau) d\tau \quad (5)$$

This can be simplified to the following expression (6).

$$\phi(t) = \frac{1}{q_{max}} \left(\frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \right) i_{noise}(t) \quad (6)$$

Since $i_{noise}(t)$ is a random signal, the output phase noise $\phi(t)$ is also a random signal. The output phase noise

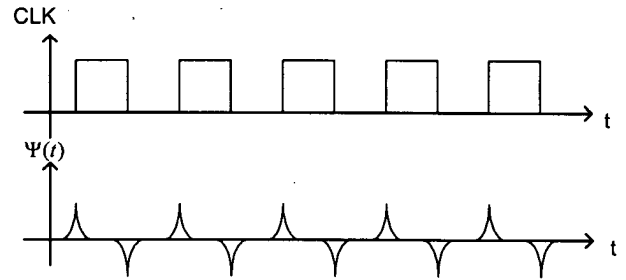


Figure 3. A Typical $\Psi(t)$ Plot

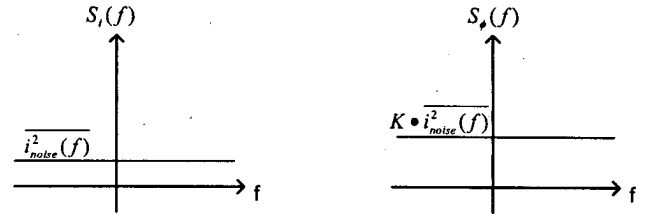


Figure 4. The input noise and the output phase noise PSD

power spectrum density (PSD) function of the random phase noise is

$$S_{\phi}(f) = \mathcal{F}[R_{\phi}(\tau)], \quad (7)$$

where \mathcal{F} is the Fourier transform and $R_{\phi}(\tau)$ is the autocorrelation function of the random signal $\phi(t)$ given by

$$R_{\phi}(\tau) = E(\phi(t)\phi(t-\tau)) \quad (8)$$

The output phase noise PSD is:

$$S_{\phi}(f) = \frac{1}{q_{max}^2} \left[\frac{c_0^2}{4} \overline{i_{noise}^2(f)} + \frac{1}{2} \sum_{n=1}^{\infty} c_n^2 \overline{i_{noise}^2(f - n f_0)} \right] \quad (9)$$

If the input noise $i_{noise}(t)$ is a white noise source, in which $\overline{i_{noise}^2(f)} = \overline{i_{noise}^2(f - n f_0)}$ is satisfied, the output phase noise power spectrum density will be as (10).

$$S_{\phi}(f) = \frac{1}{q_{max}^2} \left[\frac{c_0^2}{4} + \frac{1}{2} \sum_{n=1}^{\infty} c_n^2 \right] \overline{i_{noise}^2(f)} = K \overline{i_{noise}^2(f)} \quad (10)$$

3. DESIGN IMPLICATIONS FROM THE NOISE MODEL

From the model in section 2, the phase noise of the output clock equals to the input white noise with a scaling factor K (Figure 4). The scaling factor is represented by

$$K = \frac{1}{q_{max}^2} \left[\frac{c_0^2}{4} + \frac{1}{2} \sum_{n=1}^{\infty} c_n^2 \right]. \quad (11)$$

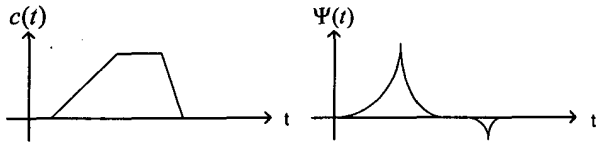


Figure 5. Unsymmetrical output clock $c(t)$ and its $\Psi(t)$

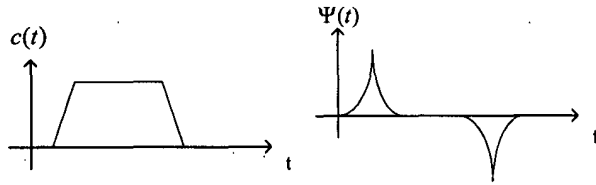


Figure 6. Symmetrical output clock $c(t)$ and its $\Psi(t)$

In order to minimize phase noise introduced by the clock buffer, K must be minimized. Firstly we can see that the factor $K \propto \frac{1}{q_{\max}^2}$, where q_{\max} is the maximum charge displacement on the noise injection node. A large q_{\max} corresponds to a large signal swing on the injection node. So a large signal swing will result in a reduction on the phase noise factor K .

K can also be reduced by minimizing the Fourier series components c_i . The coefficient c_0 , shown in (11), is the DC value of $\Psi(t)$ given by

$$c_0 = \frac{2}{T} \int_0^T \Psi(t) dt \quad (12)$$

$\Psi(t)$ is the amount of phase shift resulting from applying a unit impulse current at time t on the node. It has maximum value at the zero crossing point and has the minimum value at the peak of the output signal (Figure 3). If the output signal of the clock buffer has unsymmetrical rise time and fall time, $\Psi(t)$ will have large DC value (Figure 5). On the other hand, if the output signal of the clock buffer has symmetrical rise and fall times, $\Psi(t)$ will have a smaller DC value, i.e. smaller phase noise (Figure 6). Finally, according to Parseval's theorem:

$$\frac{c_0^2}{2} + \sum_{n=1}^{\infty} c_n^2 = \frac{2}{T} \int_0^T |\Psi(t)|^2 dt = 2\Psi_{rms}^2 \quad (13)$$

The factor K can be rewritten

$$K = \frac{1}{q_{\max}^2} \left[\frac{c_0^2}{4} + \frac{1}{2} \sum_{n=1}^{\infty} c_n^2 \right] = \frac{1}{q_{\max}^2} \Psi_{rms}^2 \quad (14)$$

From (14), reducing Ψ_{rms}^2 reduces the factor K , i.e., which minimizes the output clock phase noise. As shown in

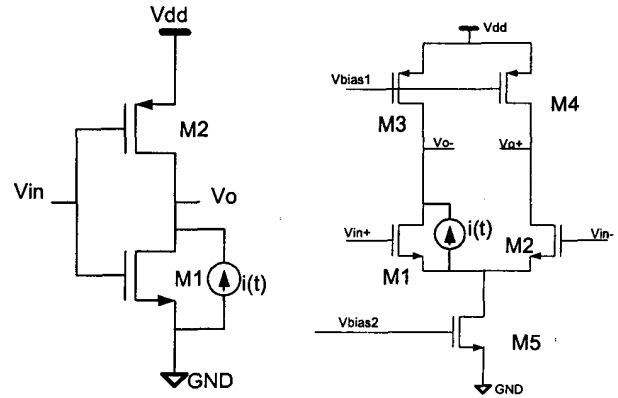


Figure 7. Clock buffers (a) Single-ended (b) Differential

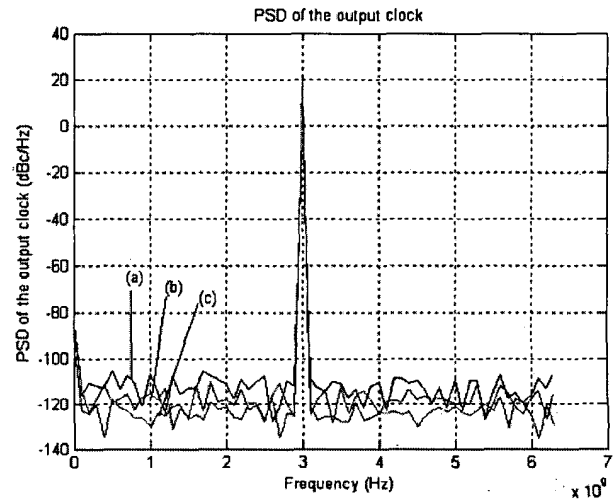


Figure 8. (a) 0.6V (b) 1.2V (c) 1.8V peak-peak 3GHz clock PSD for differential clock buffer

Figure 3, the width of each $\Psi(t)$ pulse is proportional to the rise time or fall time of the output clock. Reducing the rise and fall times of the output clock will reduce the width of $\Psi(t)$ resulting in a reduced Ψ_{rms}^2 .

In summary, the above model indicates that:

- (1) Increasing the signal swing on the noise node will reduce the phase noise degradation. A large signal swing on the noise node increases charge displacement q_{\max} across the node.
- (2) A symmetrical rise time and fall time of the output signal is desired. It will reduce the coefficient c_0 so as that reduces the output phase noise.
- (3) Small rise and fall time of the output signal is also desired. Small rise time and fall time will reduce the width of $\Psi(t)$ pulse minimizing the factor K and reducing the output phase noise.

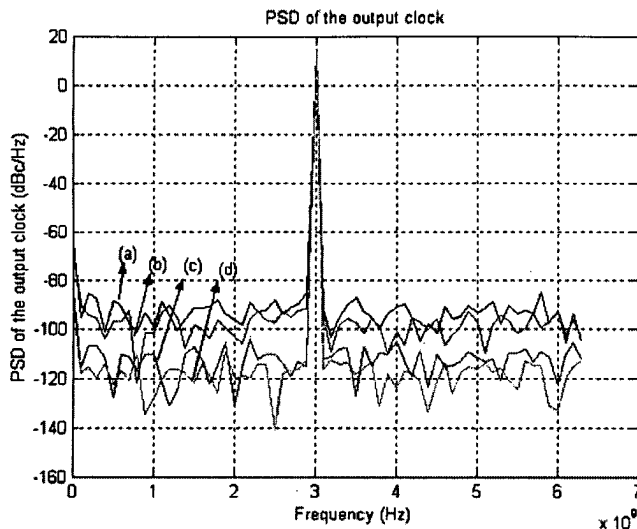


Figure 9. PSD of output clocks with different rising and falling time (a) asymmetry, slow (b) asymmetry, fast (c) symmetry, slow (d) symmetry, fast

4. SIMULATION AND MEASUREMENT RESULTS

In order to verify the accuracy of the above model, different size clock buffers were designed and fabricated in a 0.18 μ m, 1.8-V CMOS process. These clock buffers include the single-ended and differential topologies. They are shown in the Figure 7.

HSPICE simulations of phase noise resulting from the input white noise have been performed. A current source $i(t)$ across transistor M1 was added to model the input white noise. The simulation method is similar to that described in [4]. A white noise source was generated in MATLAB. The data was inputted as an HSPICE piecewise linear waveform. A transient analysis is performed and a fast Fourier transform (FFT) is computed for the output points to obtain the spectra of the phase noise. We apply a 3GHz sinusoid input signal with different swing levels (0.6V, 1.2V, 1.8V) to the clock buffer. After a transient analysis, an FFT is used to calculate the power spectrum density of the output clock signal. Figure 8 shows the PSDs of the output of clock buffer in Figure 7b. From the Figures 8, it is seen that a large signal swing does reduce the output clock noise floor. The simulation was redone by varying the rise and fall times of the clock. This was done by adjusting the size ratio (W/L) of PMOS and NMOS transistors. The results for these simulations are shown in Figure 9. From Figure 9, the design implications in items (2) and (3) are verified.

The clock buffers in Figure 7, with different transistor sizes were fabricated in 0.18 μ m, 1.8V CMOS process. The phase-noise measurements were performed using an HP 8563E spectrum analyzer (9KHz-26.5GHz) with a phase noise measurement system. The clock signals were injected with different swing levels to the different size clock

Clock buffer type	signal swing (V)	rise time (ps)	fall time (ps)	Measured phase noise (dBc/Hz)
Single end	0.6	27	27	-85.3
Single end	1.2	27	27	-100.7
Single end	1.8	27	27	-105.2
Differential	0.6	27	27	-92.4
Differential	1.2	27	27	-110.2
Differential	1.2	53	27	-87.6
Differential	1.2	12	12	-115.1
Differential	1.2	25	12	-93.7

Table I. Clock buffer phase noise measurement results

buffers and the output signal spectrum was measured. The phase noise measurement results are shown in Table I. All the reported phase noise values were measured at a 1-MHz offset from the 3GHz clock frequency.

These measurement results are compared with the simulated values and the analytical results derived in section 3. They were found to be in agreement with the measurement results.

5. CONCLUSIONS

This paper presents a phase noise model for clock buffers, an important source of phase noise for circuits operating in the gigahertz range. The model can be used to predict the phase noise introduced by clock buffers and provides better insight to the phase noise transfer mechanism in clock buffers. Based on these models, techniques for low phase noise clock buffer design were derived. The analytical results derived in this paper were shown to be in good agreement with simulations and measurements.

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