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Arbitrated address event representation digital image sensor

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Arbitrated address event representation digital image sensor

Abstract
80×60 (1/8 VGA) address event imager in 0.6 μm CMOS converts light intensity into a one-bit code (a spike). The read-out of each spike is initiated by the pixel. The dynamic range is 200 dB for a pixel and 120 dB for the array. It uses 3.4 mW at a spike rate of 200 kHz. It is capable of 8.3 k effective frames/s.

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6.3 Arbitrated Address Event Representation Digital Image Sensor

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An 80x60 (1/8 VGA) fully-arbitrated address event representation (AER) imager in a 0.6um CMOS process converts light intensity into a one-bit code (a spike). The value of the intensity is inversely proportional to the inter-spike interval. The read-out of each spike is initiated by the pixel; each pixel requests access to the output bus, and its address (x, y locations) appears at the output after arbitration [1]. Therefore, the available output bandwidth is allocated according to a pixel demand. This read-out method favors brighter pixels, minimizes power consumption by remaining dormant until data is available and supports column-parallel read-out. In contrast, a serially-scanned array allocates equal portion of the bandwidth to all pixels independent of activity and continuously dissipates power because the scanner is always active. Representing intensity in the temporal domain allows each pixel to have a large dynamic range [2], [3]. The measured dynamic range for an individual pixel is 203dB (0.008Hz - 40MHz). Similarly, under uniform illumination, the array has a dynamic range of 120dB (40Hz - 40MHz). Figure 6.3.1 summarizes the characteristics of the array. The power consumption is 3.4mW in uniform indoor light (0.1mW/cm²) and produces a mean event rate of 200kHz (41.7 effective fps). Capable of 8.3k effective fps, this imager is one of the largest dynamic range [3], lowest power [4] and fastest [5] in the literature.

Operation of the imager is divided into three parts. First the light is integrated and converted into a 1b pixel request signal, next the row and column arbitration trees select which pixel to output and finally the pixel address is encoded and the pixel is acknowledged and reset.

Because of the output-on-demand nature of the imager, the integration, read-out and reset cycle is executed asynchronously. The read-out sequence queues and outputs spikes occur according to a Poisson process, because the pixels act independently. Consequently, the probability of an address from a certain region is proportional to the light intensity in that neighborhood. This is the first reported example of a probabilistic active pixel sensor (APS), where the output activity reflects the statistics of the scene. Figure 6.3.2 shows an example of the distribution of events for a typical lab scene.

The pixel is modeled after an asynchronous address-event circuitry. Figure 6.3.3 shows the schematic of the pixel. Photons collected by an n-type photodiode are integrated on a 0.1pF capacitor, to give a slew-rate of 0.1V/µs in typical indoor light (0.1mW/cm²). Because the slew-rate can be in low light, the comparator for generating the pixel request signal must have a fast switch time with low power consumption. Using an inverter with positive feedback (Figure 6.3.4), results in 3ns switch time using only 0.084pJ (simulated). A typical inverter of similar size and speed uses about 0.18pJ. The majority of the pixel power consumption occurs during reset. To reduce reset power, the integration capacitor is disconnected from the comparator when a request is generated. The capacitor is then reset from (Vdd - Vtp) to Vdd instead of Gnd to Vdd. During reset, 3.5pJ (simulated) is used. The array, including the comparator, dissipates 100µW at Vdd and consumes only 7.3mW at 2.46MHz and consumes only 7.3mW. Figure 6.3.5 shows how the output rate per pixel, dynamic range, power and array size scale.

Imaging with this chip requires a specialized digital frame grabber, composed of a high-resolution timer (-24b) and a large frame buffer (-15MB for VGA). The timer indexes each event and compares it with the last time an event at that pixel was recorded. The difference is inversely proportional to the light intensity. The buffer must hold the latest pixel time index and the intensity value. Figure 6.3.6 shows example images recorded with the array. Note that features in the shadows can be seen using a log plot.

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References:
Figure 6.3.1: Summary of chip characteristics.

Table 6.3.1:

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Size</td>
<td>4096 x 2048</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>1 μm x 1 μm</td>
</tr>
<tr>
<td>EIR Framer</td>
<td>16 fps</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>200 dB (P@&lt;sub&gt;1&lt;/sub&gt;, 5 kHz)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Pixel Frequency Noise (VTD, Max)</td>
<td>30 MHz</td>
</tr>
<tr>
<td>Sensitivity [pW/cm&lt;sup&gt;2&lt;/sup&gt;]</td>
<td>2000</td>
</tr>
<tr>
<td>FPN (VTD/1440)</td>
<td>4 × 10&lt;sup&gt;-12&lt;/sup&gt;/V&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Max FPS</td>
<td>30 MHz</td>
</tr>
<tr>
<td>Digital Power</td>
<td>1.3 mW @ 3V Supply</td>
</tr>
<tr>
<td>Analog Power</td>
<td>0.8 mW @ 3V Supply</td>
</tr>
</tbody>
</table>

Figure 6.3.2: Poisson distribution of events. Inter-spike interval (left) and variation (right).

Figure 6.3.3: Pixel schematic.

Figure 6.3.4: Row and column arbitration architecture.

Figure 6.3.5: Scaling properties of the array. Power is computed for a fixed dynamic range.

Figure 6.3.6: Example images. Linear intensity (left) and logarithmic (right) scales.