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HIGH DYNAMIC RANGE, ARBITRATED ADDRESS EVENT REPRESENTATION DIGITAL IMAGER

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ABSTRACT

An 80 x 60 pixels arbitrated address-event imager has been designed and fabricated in a 0.6μm CMOS process. The value of the intensity is inversely proportional to the inter-spike interval and the read-out of each spike is initiated by the pixel. The available output bandwidth is allocated according to the pixel's demand, favoring brighter pixels and minimizing power consumption. The imager has a large dynamic range: 200dB for an individual pixel. The array has a dynamic range of 120dB. The power consumption is 3.4mW in uniform indoor light and a mean event rate of 200KHz (41.7 effective fps). The imager is capable of 8.3K effective fps.

1. INTRODUCTION

An 80 x 60 (1/8 VGA) fully arbitrated address event representation (AER) imager has been fabricated in a 0.6μm CMOS process. This inherently digital imager directly converts light intensity into a one-bit code (a spike). The value of the intensity is inversely proportional to the inter-spike interval. The read-out of each spike is initiated by the pixel. That is, each pixel requests access to the output bus, and its address (x and y locations) appears at the output after the arbitration trees grant it access [1]. In this way, the available output bandwidth is allocated according to a pixel's demand. This read-out method simultaneously favors brighter pixels, minimizes power consumption by remaining dormant until data is available and supports column-parallel read-out. In contrast, a serially scanned array allocates equal portion of the bandwidth to all pixels independent of activity and continuously dissipates power because the scanner is always active. Furthermore, representing intensity in the temporal domain allows each pixel to have a large dynamic range [2,3]. This approach a simple and efficient way of performing dynamic range enhancement without the use of additional circuitry by varying the integration time of each pixel based on the light intensity. This is performed using the inherently time varying scanning capability offered by address-event systems. Since the activity of the array is generated by the light intensity of the scene, and not an external scanning circuitry, the rate of collection of frames can be modulated by varying the request-acknowledge cycle time between the imager and the receiver circuitry. Section two introduces the concept of Address-Event representation. The chip architecture and imager operation is presented in section three, and the measured results and discussion in section four. A final summary describes the main features and performance of the imager.

2. ADDRESS-EVENT REPRESENTATION

The imager uses address-event representation output format. An address-event (AE) communication channel is a model of the transmission of neural information in biological systems. The imager presented here is nicknamed 'octopus retina' since it mimics the relatively simple phototransduction chain of an octopus retina [14]. The AER model trades the complexity in wiring of the biological systems for the processing speed of integrated circuits. Neurons in the human brain make up to 10^5 connections with their neighbors [6,7], a prohibitive number for integrated circuits. Nevertheless, the latter are capable of handling communication cycles that are six orders of magnitude smaller than the inter-event interval for a single neuron or cell. Thus it is possible to share this speed advantage amongst many cells, and create a single communication channel to convey all the information between two neural populations. The Address-Event is an asynchronous protocol for communication between different processing units, modeled after biological systems [1,9,10].

In the AE terminology, 'events' are communication packets that are sent from a sender to one or more receivers. For an imager, events are individual pixels reaching a threshold voltage and requesting the bus for initiating a communication with an outside receiver. An AE system is generally composed of a multitude of basic cells or elements either transmitting, receiving or transceiving data. An event has the simple form of the address of the transmitting element (hence the origin of the term address-event).

Several address-event imagers have been proposed in the literature [9,10,11,12,13] since the first devices by M. Mahowald and C. Mead [8,14]. This design targets low power consumption, high readout speeds and high dynamic range, issues that were not emphasized in earlier designs.

3. IMAGER OPERATION

3.1 IMPROVING POWER CONSUMPTION

The pixel design addresses the issue of power consumption in one of the most commonly used neuromorphic structures: the 'integrate and fire neuron'. This structure operates by integrating extremely small currents on a membrane capacitor, until the voltage exceeds some threshold. At that time, the neuron commutes its output voltage from ground to Vdd very rapidly. Later, the neuron is reset, which drains all accumulated charge

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from the membrane capacitor and the neuron is then reset after receiving an external acknowledge signal. Thus the integrate and fire neuron is a prototypical mixed signal structure, since it converts very small, slowly changing analog inputs into fast, digital signals.

The major concern with integrate and fire neurons is its power consumption. A digital inverter consumes about 0.06pJ (40uW x 3ns x 0.5) per on-transition (rising input, falling output) and about 0.18pJ (120uW x 3ns x 0.5) per off-transition (falling input, rising output). Note that a factor of 0.5 is a waveform correction factor, and the input waveform had an arbitrarily specified risetime and falltime of 3ns (slew rate of approximately 1V/ns). However, in a typical integrate and fire neuron, the input slew rate is six orders of magnitude slower, or 1V/ms, during the charging phase, although the reset phase is usually faster. This means that the input voltage is kept in the high-power region where there is current path between the supplies for a much longer period than is the case for an inverter in a digital system. Even with improvements, the power consumption of integrate and fire neurons is about 10,000 to 1,000,000 times greater than that of a simple inverter.

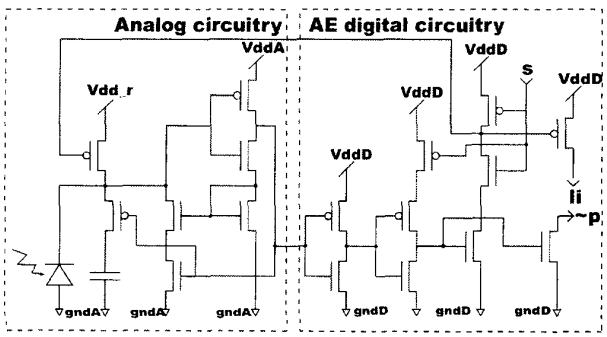

Figure 1: Pixel Schematic.

These power requirements are prohibitive when large neuromorphic systems are to be constructed on a chip. In fact low power consumption is one of the main advantages of analog biological-modeled systems. Furthermore the surges in power consumption caused by digital transition degrade the performance of the sensitive analog circuits if the analog and digital supply are not properly separated.

3.2 PIXEL OPERATION

The proposed pixel is modeled after an active pixel sensor (APS) [17], but also includes circuitry that generates the address event request and resets the APS when the request is acknowledged. The operation of the imager is divided into three main phases. First the light is integrated and converted into a 1-b pixel request signal, next the row and column arbitration trees select which pixel to output and finally the pixel's address is encoded, output and the pixel acknowledged and reset. Figure 1 shows the schematic of the pixel. Photons collected by an n-type photodiode are integrated on a 0.1pF capacitor, to give a slew-rate of 0.1V/ms in typical indoor light (0.1mW/cm^2). Because the slew-rate can be very small in low light, the comparator for generating the pixel request signal must have a fast switching time with low power consumption. Using an inverter with positive feedback, shown in figure 1, we obtained a switch time of 3ns while using only 0.084pJ (simulated). A typical inverter of similar size and speed uses about 0.18pJ (as stated in section 3.1). The majority of the pixel's power consumption occurs during reset. To reduce reset power, the integration capacitor is disconnected from the comparator when a request is generated. The capacitor is then reset from *~(Vdd – Vtp)* to *Vdd* instead of *Gnd* to *Vdd*. During reset, 3.88pJ (simulated) is used.

The array, including the comparator, dissipates 100μW @ *Vdd_analog* = 2.75V running at 200KHz in uniform room light (~0.1mW/cm^2). When imaging a typical indoor scene, the analog power consumption drops to below 10μW, since the mean firing rate decreases.

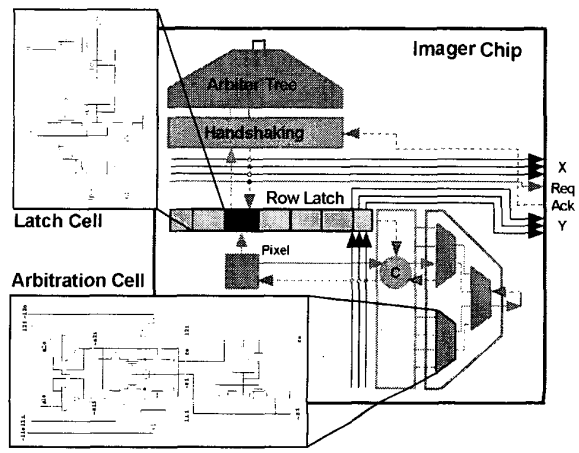

Figure 2: Row and column arbitration architecture.

The digital circuit for generating the pixel request and receiving an acknowledge/reset are also shown in the right part of figure 1. When the comparator is triggered, a row request, *~p*, is generated. The row arbitrator picks one active row. The selected row is copied into a buffer sitting above the array. The signal *li* indicates which pixel in the row has issued a request. This buffer provides a pixel access speed-up and improved parallelism by realizing a pipelined read-out scheme. Once copied, the entire row is acknowledged/reset (signal *s*), the row address is generated by a ROM, and photon integration starts anew. Column arbitration is performed on the buffered row. The arbitration tree selects the active elements in the buffer, computes and outputs their addresses before clearing the buffer. A new active row is obtained when the buffer is clear. Performing column arbitration on the buffered row also improves read-out speed by eliminating the large capacitance associated with the column lines. This capacitance is encountered when arbitration is

performed within the whole array. Figure 2 shows the architecture of the row and column arbitration circuits.

The main draw back of this approach is the complexity of the digital frame grabber required (pixel size, FPN and power consumption can be reduced with more careful circuit designs). To count all the spikes produced by the array, a high-resolution timer (~24 bits) and a large frame buffer are required (~15MB for VGA). The timer indexes each event and compares it with the last time an event at that pixel was recorded. The difference is inversely proportional to the light intensity. The buffer must hold the latest pixel time index and the intensity value. Figure 3 shows example images recorded with the array. Note that features in the shadows can be seen using a log plot.

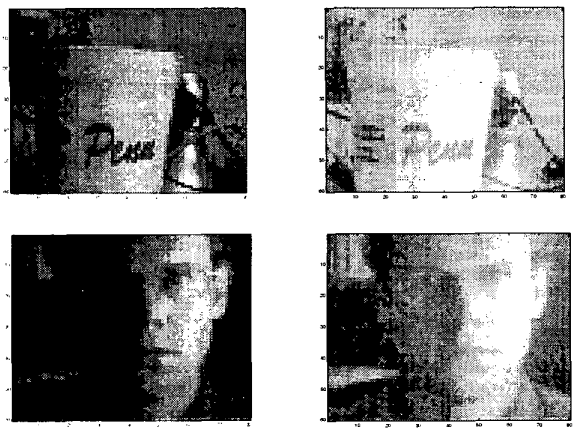

Figure 3: Example images. Linear intensity (left) and log (right) scales.

4. RESULTS AND DISCUSSION

4.1 IMAGER STATISTICS

Because of the output-on-demand nature of our imager, the integration, read-out and reset cycle is executed asynchronously. The read-out sequence queues and outputs spikes occurring according to a Poisson process, since the pixels act independently. Consequently, the probability of an address from a certain region is proportional to the light intensity in that neighborhood. This is the first reported example of a probabilistic APS, where the output activity reflects the statistics of the scene. Figure 4 shows an example of the distribution of events for a typical lab scene. The left part of figure 4 suggests a clear exponential behavior for inter-event timing as the parameters extracted are 790 as intercept and -0.01446 as exponent multiplier.

The right part of picture 4 shows the inter-event timings of a single pixel. The spiking element, while viewing the same scene with constant illumination, produces a highly deterministic pattern of events. The mean spiking rate is much higher than its standard deviation. Statistical differences in cycle times are due to the arbitration queuing system at the output of the imager. When multiple pixels request the bus, the service time varies, which in turn changes the inter-spike interval [1]. The cycle time statistics for events generated by pixel (30,30) of the higher picture in figure 3 show a mean of 0.54527 and standard deviation of 0.0580.

This data in figure 4 was collected from all the 60 by 80 photodiode cells in the array collecting events generated by Octopus Retina while observing a scene. A Tektronix TLA714 Logic Analyzer with a 2 Ghz bandwidth was used.

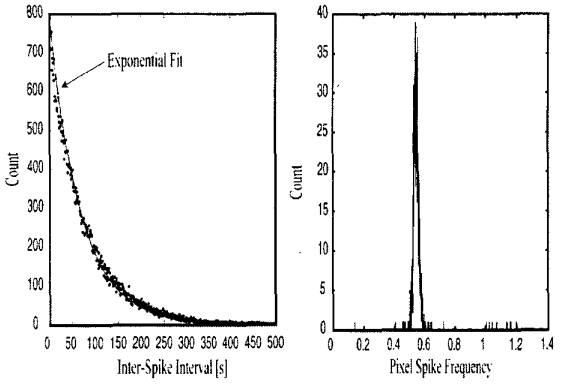

Figure 4: Poisson distribution of events. Inter-spike interval (left) and variation (right).

4.2 IMAGER PERFORMANCE

The measured dynamic range for an individual pixel is 200dB (0.008Hz – 40MHz). Similarly, under uniform illumination, the array has a dynamic range of 120dB (40Hz – 40MHz). Table I summarizes the characteristics of the array. The power consumption is 3.4mW in uniform indoor light (0.1 mW/cm2) and produces a mean event rate of 200KHz (41.7 effective fps). Capable of 8.3K effective fps, this imager is one of the largest dynamic range [3], lowest power [4] and fastest [5] in the literature. The relationship between event (output) frequency and power consumption is given by P[mW] = 1.7F [MHz] + 3.1 (empirical fit), where F is the event frequency. The static dissipation is produced by the pseudo-CMOS logic used in this design. At full speed (40MHz and 8.3Kfps), and maximum array dynamic range (6 decades), the power consumption will be 71mW. Normal operation produces events at a maximum of 4MHz (0.8Kfps), for a dynamic range of 5 decades, while consuming 10mW. A full VGA with 3 decades of dynamic range operates at 2.46MHz and consumes only 7.3mW. Figure 5 shows how the output rate per pixel, dynamic range, power and array size scales.

5. SUMMARY

An 80 x 60 pixels fully arbitrated address-event imager was fabricated and tested. The imager provides a very large dynamic range of 120dB, a low power consumption of 3.4mW and is

capable of 8.3K effective fps. The digital power usage can be further improved by removing all pseudo-MOS logic devices.

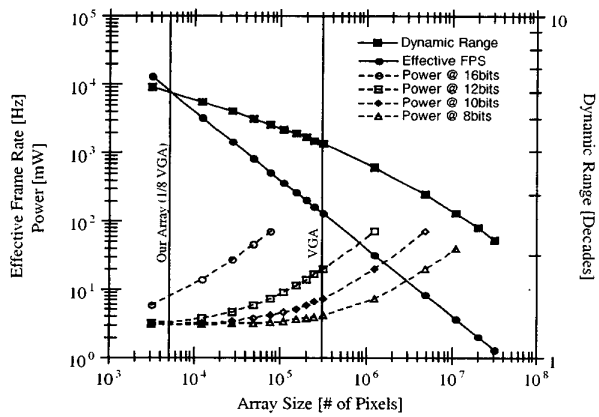

Figure 5: Scaling properties of the array. Power is computed for a fixed dynamic range.

Technology	0.6μm 3M CMOS
Array Size	80 (H) x 60(V)
Pixel Size	32μm x 30μm
Fill Factor	14%
Dynamic Range	200dB (Pix.) 120dB (Array)
Bandwidth	8mHz – 40MHz (Pix.) 40Hz-40MHz (Array)
Pixel Frequency Jitter (STD/Max)	$6x10^{-4}$ %
Sensitivity [Hz/mW/cm^2]	$2x10^6$ (Array) 42 (Pix.)
FPN (STD/Mean pixel-pixel) @ 0.1 mW/cm^2	4%
Max. FPS	8.3K (effective)
Digital Power @ 2.9V Supply	(1.7*F[MHz]*+3.1) mW 3.4mW @ 0.1mW/cm^2
Analog Power @ 2.7V Supply	< 10μW for scene @ 0.1mW/cm^2

Table I: Summary of chip characteristics.

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