May 2002

On-off differential current-mode circuits for Gabor-type spatial filtering

Bertram E. Shi  
*Hong Kong University of Science and Technology*

Thomas Yu Wing Choi  
*Hong Kong University of Science and Technology*

Kwabena A. Boahen  
*University of Pennsylvania*, boahen@seas.upenn.edu

Follow this and additional works at: [http://repository.upenn.edu/be_papers](http://repository.upenn.edu/be_papers)

Recommended Citation

Shi, B. E., Choi, T. Y., & Boahen, K. A. (2002). On-off differential current-mode circuits for Gabor-type spatial filtering. Retrieved from [http://repository.upenn.edu/be_papers/22](http://repository.upenn.edu/be_papers/22)

Publisher URL: [http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=21785&page=12](http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=21785&page=12)

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of the University of Pennsylvania's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

This paper is posted at ScholarlyCommons. [http://repository.upenn.edu/be_papers/22](http://repository.upenn.edu/be_papers/22)  
For more information, please contact libraryrepository@pobox.upenn.edu.
On-off differential current-mode circuits for Gabor-type spatial filtering

Abstract
We describe a current-mode circuit for Gabor-type image filtering which uses a differential representation where positive (on) and negative (off) signals are encoded using separate channels. Previous current-mode implementations represented positive and negative signals as variations around a constant bias at every pixel. However, this bias current has several disadvantages. First, variations in it introduce significant additive fixed pattern noise to the output. Second, it dissipates power even with zero input. Third, if the output is encoded using the Address Event Representation, the bias current sets up a quiescent firing rate which loads the bus. The architecture proposed here alleviates these problems since a zero signal is encoded as nearly zero current in both channels. On the other hand, the transistor count and the address space are doubled. Measurements from a 1 by 25 pixel array with a cell size of 64 µm by 540 µm was fabricated in the AMI 1.5 µm process available through MOSIS. Quiescent power dissipation was 5 µW total.

Comments
Publisher URL: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=21785&page=12

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of the University of Pennsylvania’s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
On-Off Differential Current-mode Circuits for Gabor-type Spatial Filtering

Bertram E. SHI1, Thomas Yu Wing CHO1 and Kwabena BOAHEN2
1Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong, {cebert, cethomas}@ee.ust.hk
2Department of Bioengineering, University of Pennsylvania, Philadelphia, PA 19104-6392, kwabena@neuroengineering.upenn.edu

ABSTRACT
We describe a current-mode circuit for Gabor-type image filtering which uses a differential representation where positive (on) and negative (off) signals are encoded using separate channels. Previous current-mode implementations represented positive and negative signals as variations around a constant bias at every pixel. However, this bias current has several disadvantages. First, variations in it introduce significant additive fixed pattern noise to the output. Second, it dissipates power even with zero input. Third, if the output is encoded using the Address Event Representation, the bias current sets up a quiescent firing rate which loads the bus. The architecture proposed here alleviates these problems since a zero signal is encoded as nearly zero current in both channels. On the other hand, the transistor count and the address space are doubled. Measurements from a 1 by 25 pixel array with a cell size of 64um by 540um was fabricated in the AMI 1.5um process available through MOSIS. Quiescent power dissipation was 5uW total.

1. INTRODUCTION
2D Gabor filters have been used to model the receptive field profiles of orientation selective neurons in the visual cortex. These filters have also been used as front end pre-processing stages for applications such as image motion analysis, and texture and face recognition. Typically, the input image is convolved with a set of Gabor filters tuned to different orientations, where the magnitude of the filter output is large where the filter orientation matches that in the input image.

The impulse response of a Gabor filter is a complex exponential waveform modulated by a Gaussian function. A Gabor-type filter has an impulse response which is a complex exponential modulated by any low pass function, e.g. in 1D

\[ h(n) = H_{\Omega} \frac{\Delta \Omega}{2} e^{-\Delta \Omega \delta \theta / \Omega} \]

This filter is tuned to respond maximally to a spatial frequency \( \Omega \) with gain \( H_{\Omega} > 0 \) and 6dB half bandwidth \( \Delta \Omega > 0 \). A focal plane implementation of an analog VLSI current mode circuit implementing Gabor-type spatial filters with impulse response (1) was reported in [1], where the real and complex parts of the filter output were each represented as the variation in a single current around a quiescent bias value. However, this bias current has several disadvantages. First, variations in this bias current due to mismatch add significant fixed pattern noise to the output. In [1], the measured fixed pattern noise in the output was 26%-38% of the bias current. Second, the array dissipates power even with zero input. Finally, if the array output is encoded using spiking neuron circuits for inter-chip transmission via the Address Event Representation (AER) protocol, the bias contributes to a mean spiking rate which loads the AER bus even with a zero input signal.

2. SINGLE CURRENT ARCHITECTURE
In this section, we briefly review the current mode Gabor-type spatial filtering architectures which used a single current to represent each signal[1]. For clarity, we assume 1D images throughout the paper and refer to [1] for the extension to 2D.

The filter output can be expressed as the solution to the following set of equations:

\[ \begin{align*}
0 &= \alpha_1 i(n-1) - (1 + 2 \alpha_2) i(n) + \alpha_2 \delta i(n+1) \\
&- \alpha_1 i(n-1) + \alpha_2 i(n) + u(n) \\
0 &= \alpha_1 i(n-1) - (1 + 2 \alpha_2) i(n) + \alpha_2 i(n+1) \\
&+ \alpha_1 i(n-1) - \alpha_2 i(n+1)
\end{align*} \]

(2)

where \( n \) is the pixel index, \( i(n) \) and \( \delta i(n) \) are the real and imaginary parts of \( i(n) \) and

\[ \alpha_1 = \frac{\cos \Omega}{(\Delta \Omega)^2 H_{\Omega}} \quad \alpha_2 = \frac{\sin \Omega}{(\Delta \Omega)^2 H_{\Omega}} \quad H_{\Omega} = 1 + \frac{2 - 2 \cos \Omega}{(\Delta \Omega)^2} \]

A block diagram of a current mode circuit implementation of (2) as well as transistor level schematics of each block are shown in Figure 1. The larger blocks detailed in Figure 1(b) implement the first lines of each equation in (2) using transistors operating as "pseudo-resistors" or "diffusors"[2][3]. The bias currents \( I_{\text{bias}} \) are added to each node because the filter output can be both positive and negative, but the diffusion circuit in Figure 1(b) operates correctly only if all cur-
rents are positive. The difference between $V_h$ and $V_v$ controls the value of $\alpha_1$. The cross couplings between the real and imaginary parts of the filter response are implemented using current amplifiers as shown in Figure 1(c).

The gain $\alpha_2$ depends exponentially on the difference between source voltages $V_{s1}$ and $V_{s2}$. The filter can be tuned to any desired values of $0 \leq \Omega \leq \pi/2$ and $\Delta \Omega > 0$ adjusting the voltages $V_h, V_v, V_{s1}$ and $V_{s2}$.

3. DIFFERENTIAL ARCHITECTURES

3.1 Linear Differential Architecture

A simple linear differential architecture can be obtained by defining the input and outputs of the filter as the differences between two signals: $u(n) = u_+(n) - u_-(n)$, $i_r(n) = i_r(n) - i_r(n)$ and $i_i(n) = i_i(n) - i_i(n)$ where the subscripts + and - denote the positive and negative parts. Consider the following set of equations:

$$
0 = \alpha_1 i_r(n-1) - (1 + 2 \alpha_1) i_r(n) + \alpha_1 i_i(n+1) + \alpha_2 i_i(n-1) + \alpha_2 i_i(n) + u_+(n)
$$

$$
0 = \alpha_1 i_r(n-1) - (1 + 2 \alpha_1) i_i(n) + \alpha_1 i_i(n+1) + \alpha_2 i_i(n-1) + \alpha_2 i_i(n) + u_-(n)
$$

$$
0 = \alpha_1 i_r(n-1) - (1 + 2 \alpha_1) i_i(n) + \alpha_1 i_i(n+1) + \alpha_2 i_i(n-1) + \alpha_2 i_i(n) + u_+(n)
$$

$$
0 = \alpha_1 i_r(n-1) - (1 + 2 \alpha_1) i_i(n) + \alpha_1 i_i(n+1) + \alpha_2 i_i(n-1) + \alpha_2 i_i(n) + u_-(n)
$$

which can be implemented using the block diagram shown in Figure 2. By eliminating the negative gains, we ensure

![Fig. 1: (a) A block diagram of the circuit architecture implementing equation (2). Each signal $u$, $i_r$, and $i_i$ is a spatially distributed array representing the input and output images. The $z$ operator represents a spatial shift. (b,c) Transistor level implementations of the blocks in (a).](image)

![Fig. 2: System level implementation of equation (3) where each variable is encoded differentially. The circuit implementations of each block are similar to those shown in Figure 1, except the circuits are doubled to process the positive and negative components separately.](image)
that the currents in the diffuser network are always positive and eliminate the need for the constant bias current. However, this adversely affects the stability of the array, as shown below.

By subtracting the second equation from the first and the fourth equation from the third, we can verify that \( i_{n}(n) \) and \( i_{n}(n) \) satisfy (2). For a complete characterization of the output, we must also consider the common mode response. Define the common mode components of the input to be
\[
u_{c}(n) = 0.5(u_{c}(n) + u_{c}(n))
\]
and similarly for \( i_{n}(n) \) and \( i_{n}(n) \). Adding the first two and second two equations in (3), we obtain
\[
\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \alpha_1 \alpha_2 \\ \alpha_2 \alpha_1 \end{bmatrix} \begin{bmatrix} i_{n}(n-1) \\ i_{n}(n-1) \end{bmatrix} - \begin{bmatrix} 1 + 2\alpha_1 & 0 \\ 0 & 1 + 2\alpha_1 \end{bmatrix} \begin{bmatrix} i_{n}(n) \\ i_{n}(n) \end{bmatrix}
\]
\[
+ \begin{bmatrix} \alpha_1 \alpha_2 \\ \alpha_2 \alpha_1 \end{bmatrix} \begin{bmatrix} i_{c}(n+1) \\ i_{c}(n+1) \end{bmatrix} + \begin{bmatrix} u_{c}(n) \\ 0 \end{bmatrix}
\]
(4)

Assume an infinite array and define
\[
U_{c}(\omega_{n}) = \sum_{n} u_{c}(n) e^{-j\omega_{n}n}
\]
for \( \omega_{n} \in [-\pi, \pi] \) to be the spatial Discrete Fourier transform of the input \( u(n) \) and similarly for \( I_{c}(\omega_{n}) \) and \( I_{c}(\omega_{n}) \). Taking the discrete Fourier transform of both sides of (4), we obtain
\[
\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \mathcal{A}(\omega_{n}) \end{bmatrix} \begin{bmatrix} I_{c}(\omega_{n}) \\ 0 \end{bmatrix} + \begin{bmatrix} U_{c}(\omega_{n}) \end{bmatrix}
\]
where
\[
\mathcal{A}(\omega_{n}) = \begin{bmatrix} 1 + 2\alpha_1 - 2\alpha_2 \cos\omega_{n} & -2\alpha_2 \cos\omega_{n} \\ -2\alpha_2 \cos\omega_{n} & 1 + 2\alpha_1 - 2\alpha_2 \cos\omega_{n} \end{bmatrix}
\]
The common mode component of the response will be stable as long as all of the eigenvalues of the \( \mathcal{A}(\omega_{n}) \) matrix are positive for all \( \omega_{n} \). The eigenvalues of \( \mathcal{A}(\omega_{n}) \) are
\[
s = 1 + 2\alpha_1 - 2(\alpha_1 \pm \alpha_2 \cos\omega_{n})
\]
which are positive for all \( \omega_{n} \) if and only if \( |\alpha_2| < 1/2 \) and \( |\alpha_2| < 2\alpha_1 + 1/2 \). If the \( \alpha_1 \) term is implemented using diffusers as suggested here, then \( \alpha_3 > 0 \) and only the first inequality is relevant. Unfortunately this excludes a large proportion of the filter parameter space, corresponding to sharp filter tunings. See Figure 3.

### 3.2 Differential On-Off Architectures

To avoid the instability in the common mode component, we add circuits which limit the common mode signals. Each of these circuits takes two unidirectional input currents and outputs two unidirectional currents where the difference between the two output currents is the same as the difference between the two input currents, but one of the output currents is close to zero. Mathematically,
\[
\begin{align*}
i_{out+} &= i_{in+} - \min(i_{in+}, i_{in}) \\
i_{out-} &= i_{in+} - \min(i_{in+}, i_{in})
\end{align*}
\]
A transistor circuit which approximates this function is shown in Figure 4. This circuit limits the common mode component of the signal to one half the magnitude of the differential component.

Figure 5 shows block diagrams of one possible differential implementation using this on/off circuit where the on-off circuit is applied at the input of the diffuser network. A non differential version of this is analysed in [2]. Because positive input current flows out of the circuit, the spatial shift circuits with current gain are implemented using the circuits shown on the right hand side of Figure 1(c).

### 4. EXPERIMENTAL RESULTS

A 1x25 pixel array was fabricated using the architecture shown in Figure 5 using the AMI 1.5um process available thorough MOSIS. The layout of the Gabor processing circuits occupied 64um x 540um. The layout was deliberately
made narrow and tall maximize the number of pixels which could be implemented on the 2.2mm by 2.2mm die. Quiescent power dissipation was 5uW total (200nW per pixel) at a power supply voltage of 5V.

Figure 6 shows the measured results from the array to a spatial impulse input. The array is tuned to $\Omega = 0.3\pi$ and $\Delta\Omega = 0.5\Omega$, which is in the unstable region of the linear differential architecture, indicating that the on/off circuit is effective in suppressing the instability of the linear architecture.

5. CONCLUSION

We have described a differential current mode implementation of Gabor-type spatial filtering which alleviates some of the problems encountered with a single ended architecture, at the expense of doubling the hardware complexity. Because the common mode response of a simple linear differential implementation is unstable for a large part of the desired filter parameter space, it is necessary to add a nonlinear element to limit the common mode response. Measured results from a 1x25 pixel array confirm proper operation.

ACKNOWLEDGMENTS

This work was supported by the Hong Kong Research Grants Council under grants HKUST6216/98E and HKUST6218/01E.

REFERENCES

