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Loop With 30MHz to 2GHz Locking  
Range and  $\pm 35$ ps Jitter

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# FULLY INTEGRATED CMOS PHASE-LOCKED LOOP WITH 30MHZ TO 2GHZ LOCKING RANGE AND $\pm 35$ PS JITTER

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**Abstract** A fully integrated phase-locked loop (PLL) fabricated in a 0.24 $\mu$ m, 2.5v digital CMOS technology is described. The PLL is intended for use in multi-gigabit-per-second clock recovery circuits in fiber-optic communication chip. This PLL first time achieved a very large locking range measured to be from 30MHz up to 2GHz in 0.24 $\mu$ m CMOS technology. Also it has very low peak-to-peak jitter less than  $\pm 35$ ps at 1.25GHz output frequency.

## 1. INTRODUCTION

In recent years, there has been a significant research effort in the area of high-speed electronics for communication. High speeds are required in order to take full advantage of the extremely broadband capabilities of optical fibers. At the same time, the old communication protocols that use different low speeds are still being widely used. In order to lower the cost and to be flexible for the different protocols, a large locking range PLL clock generator is highly needed. In particular, fully integrated CMOS solutions are sought for practical systems to reduce cost and improve reliability. Although a lot of different speed PLLs have been reported recently [1][2][3][4][8], the large locking range from 30 MHz to 2GHz CMOS PLL has not been seen in 0.24 $\mu$ m CMOS technology. Also, in many applications, the generated clock signals are used to drive sampling circuits in which the random variation of the sampling instant, or jitter is a critical performance parameter. The low noise jitter PLL is becoming more and more important.

In this paper, a fully integrated PLL, with a large locking range from 30 MHz to 2 GHz, peak-to-peak jitter noise  $\pm 35$ ps at 1.25GHz output frequency is described. In section 2, a newly invented dual-looped architecture is described. In section 3, the design of the voltage control

oscillator (VCO) with large tuning range and low jitter noise is presented. The other circuits that make up the completed PLL, such as PFD and charge pump are described in section 4. Finally, measurements and experimental results of the chip are given in section 5 and 6.

## 2. DUAL-LOOPED PLL ARCHITECTURE

A block diagram of the classical single-looped PLL is shown in figure 1(a). In order to increase the locking range and reduce the output clock jitter, a newly invented dual-looped architecture is used in our design. The block diagram of this new invented architecture is depicted in figure 1(b).

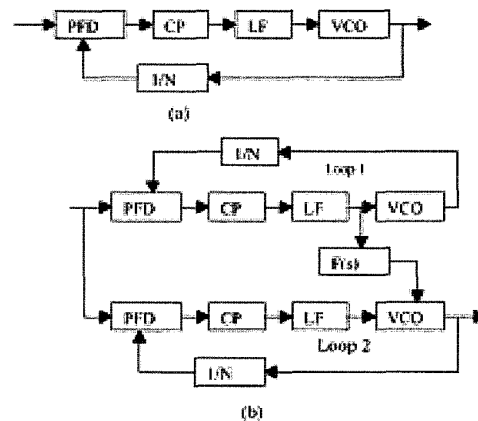


Figure1 (a) Classical single-looped PLL  
(b) New dual-looped PLL architecture

The new dual-looped PLL architecture consists of two classical single-looped PLLs, loop1 and loop2. Loop1 is identical to the classical single-looped architecture, as noted in Garden's work [5]. Loop2 is however different by having an extra added control from Loop1. The control signals of the VCO in the loop2 are taken from



signal from the loop1. This DC control voltage sets the output frequency of the loop 2 close to the locked frequency. And the other control current source is used to finely tune the output frequency to the locked frequency by the loop2 itself.

For N-stage ring oscillator, the gain for each delay cell must satisfy the following condition in order to oscillate.

$$A_v = g_m R \geq \sqrt{1 + \tan^2 \frac{\pi}{N}}$$

In the design of the bias circuit, a large tuning range requires that the load impedance be adjusted inversely proportional to the  $g_m$ . The load impedance R will be changed while we adjust the tail currents by the biased circuit. The goal is to make the  $A_v$  almost constant in the whole tuning range. Also the replica bias circuit is used to get the constant swing. The bias circuit is depicted in figure 3.

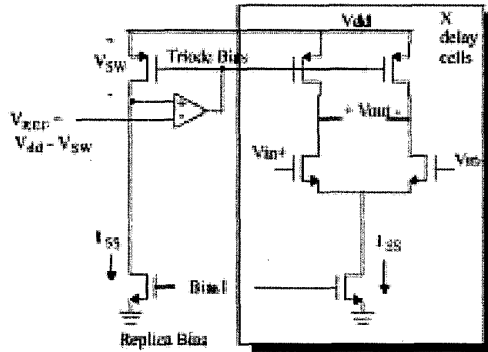


Figure 3. Simplified replica biasing circuit

#### 4. OTHER PLL CIRCUITS

The Phase-Frequency Detector (PFD) used is shown in figure 4. The “dead zone” problem is avoided by adding delays in the loop. The PFD generates two minimum length UP and DOWN pulses, even when the compared waveforms are perfectly synchronized. Those pulses are identical in length, so the up and down currents cancel each other. When the input reference and the feedback clock are not perfectly synchronized, PFD will generate unequal UP and DOWN pulse and let the charge pump to charge the loop filter to adjust the feedback clock phase or frequency.

The charge-pump used is shown in figure 5 [9]. Since the PFD eliminates the “dead zone” by

turning both sources on at the same time, a current mismatch between the sources can inject extra noise to the output control node. To avoid variations of the output current due to the output voltage, high-impedance cascode current sources are used.

When the pulse controlling a source is low, normally the source would be turned off. This may cause charge injection at the switching time and slow response. To avoid this problem, the currents are redirected to the output of a unity gain buffer kept at the same voltage as the output of the loop filter. This prevents the current fluctuations that are due to the finite output impedance of the current sources.

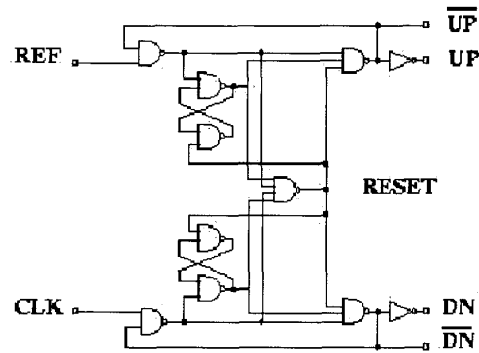


Figure 4: PFD block diagram

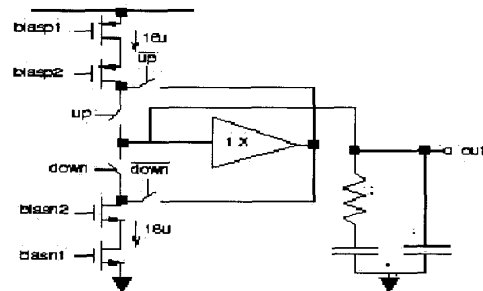


Figure 5. Charge pump circuit

#### 5. MEASURED RESULTS

The following table shows the measured performance of the PLL when functioning with the output frequency running at 1.25GHz.

Peak-to peak jitter	$\pm 35\text{ps}$
Acquisition time	$<15\mu\text{s}$
Phase margin:	$>70^\circ$
Power dissipation:	$<300\text{mw}$
Die area:	$350 \times 800 \mu\text{m}^2$

Figure 6 shows the digital oscilloscope display of the eye diagram of the output clock at 1.25GHz superimposed with a histogram of its jitter. The measured VCO range of the PLL is shown in Figure 7. The range, which is as low as 30 MHz and as high as 2 GHz, has been demonstrated. The figure 8 shows the die micrograph of the PLL.

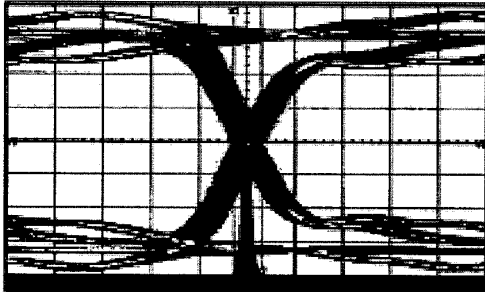


Figure 6 Eye diagram with histogram of jitter

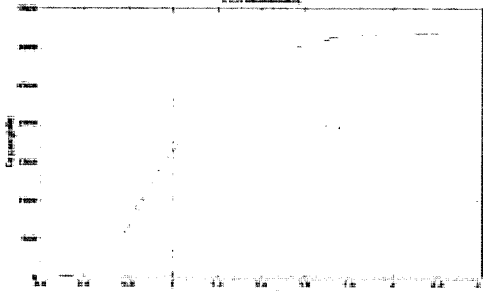


Figure 7. VCO tuning range

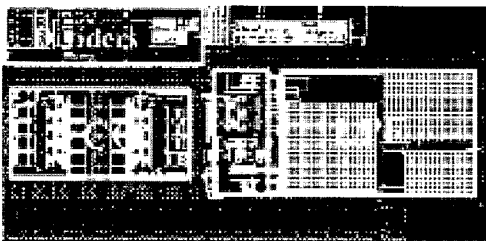


Figure 8. The micrograph of PLL ( $345 \times 803 \mu\text{m}^2$ )

## 6. CONCLUSIONS

A large locking ranges from 30 MHz to 2 GHz PLL has been developed in a digital 0.24um, 2.5V CMOS technology. It is the first time that such a large locking range has been obtained in this technology. The PLL can operate as a part of a noisy logic CMOS chip and is designed to address a wide range of applications. It is fully integrated and has demonstrate lower peak-to-peak of  $\pm 35\text{ps}$  jitter at 1.25GHz output frequency.

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