

# GBOPCAD: A Synthesis Tool for High-Performance Gain-Boosted Opamp Design

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**Abstract**—A systematic design methodology for high-performance gain-boosted opamps (GBOs) is presented. The methodology allows the optimization of the GBO in terms of ac response and settling performance and is incorporated into an automatic computer-aided design (CAD) tool, called GBOPCAD. Analytic equations and heuristics are first used by GBOPCAD to obtain a sizing solution close to the global optimum. Then, simulated annealings are used by GBOPCAD to find the global optimum. A sample opamp is designed by this tool in a 0.6- $\mu\text{m}$  CMOS process. It achieves a dc gain of 80 dB, a unity-gain bandwidth of 836 MHz with 60° phase margin and a 0.0244% settling time of 5 ns. The sample/hold front-end of a 12-bit 50-MSample/s analog–digital converter was implemented with this opamp. It achieves a signal-to-noise ratio of 81.9 dB for a 8.1-MHz input signal.

**Index Terms**—Doublet, equation based, gain boost, gain-boosted opamp computer-aided design (GBOPCAD), global optimum, stability, high-speed opamp, opamp synthesis, sample/hold (S/H) front-end, simulated annealing (SA).

## I. INTRODUCTION

THE operational amplifier is one of the most fundamental components in analog integrated circuit design. It is the critical component that, in most cases, is responsible for the performance of switch-capacitor circuits. The demands for high-performance CMOS analog circuits increased dramatically in recent years, especially for digital–analog interface circuits [1], due to the emergence of system-on-chip (SoC). In recent years, considerable efforts have been spent on the design of CMOS analog–digital converters (ADCs) with higher sampling rates and resolution [2]–[4]. One of the essential tasks in all these efforts is to provide a high-performance opamp with high gain and bandwidth, and fast settling time.

High-speed opamps use only one stage to reduce the parasitics in order to achieve a high bandwidth. Telescopic opamps and folded-cascode opamps are commonly used for this purpose [19]. In order to achieve a high gain with high bandwidth, a gain boosting technique [5] is normally incorporated by exploiting the principle of the regulated-cascode stage [6]. However, the existence of a doublet can unfavorably delay the settling process of the gain-boosted opamp (GBO) [5], [7]. On the other hand,

the effort of reducing the effect of the doublet can raise a stability problem. Our work will show that the complex conjugate pole pair reported in [8] and [9] eventually pushes the system into instability. Therefore, it is necessary to optimize the design of GBO for its transient performance.

Many computer-aided design (CAD) tools [10]–[17] have been developed for analog circuit synthesis, especially for opamp synthesis. A generic analog synthesis CAD tool usually includes separate steps of topology selection and circuit sizing. Some tools, such as DARWIN [10], uses genetic algorithms to combine these two steps during the synthesis. However, the overhead of computation time would be tremendously increased, in order to find a real globally optimal solution. Besides, a small number of possible topology candidates can be chosen relatively easy by an experienced synthesis system, based on the coded heuristics and the previous designs, just as experienced circuit designers do. Therefore, we believe that a system including individual sizing routines for different topologies, with a topology selection process based on heuristics, is a more viable choice for practical analog synthesis CAD tools.

In terms of circuit sizing, three essential issues, which are accuracy, global optimality and computation time, have to be properly addressed in the design of practical analog synthesis CAD tools.

Equation-based approaches [11]–[14] rely heavily on simplifications of circuit equations and device models. Using special optimization techniques for equations, such as geometric programming in [11], these tools can solve the optimization problem in minutes. However, although the simplified equations can show the first or second order behavior of circuits, higher order effects, which can be rather important for CMOS processes in the deep-micro range, are usually neglected. As a result, the optimal solution out of equation-based CAD tools can deviate substantially from the real circuit optimum. In order to obtain solutions with better accuracy, a long preparatory period is usually required to derive better-performing equations, which undermines the justification of this type of approach.

Simulation-based approaches [15]–[17] resolve the accuracy problem by directly using SPICE for circuit evaluation. Tools, like DELIGHT.SPICE in [15], use gradient-based optimization techniques, which makes them capable of finding only local optimal solutions. In order to find the global optimum for circuits, simulated annealing (SA) is used in [16] and [17]. As introduced in [18], in theory, with sufficiently large annealing times, SA is able to find the global optimum within the design space, regardless of the initial condition. However, the design space is usually rather complicated for most real design problems. It is difficult to design an adaptation process for plain SA,

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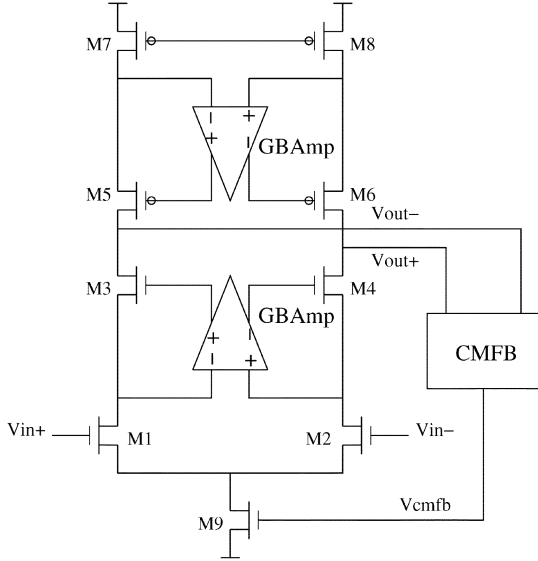


Fig. 1. TGBOP structure.

without any knowledge of the circuit, to settle to the exact global optimum, which leads to the pessimistic assertion in [11] about SA. In order to increase the chance of reaching the global optimum, long annealing runs are used by these CAD tools.

A new automatic synthesis tool, GBOPCAD, is proposed in this paper by combining the characteristics of equation-based approaches and that of the simulation-based approaches, so as to gain the benefits of both methods, while avoiding their shortcomings. In our approach, a good sizing solution, which is close to the global optimum, is found by using algorithms based on equations and heuristics at first. SA is then carried out on the basis of this good initial condition, which enables the tool a higher probability of reaching the global optimum. GBOPCAD is currently a synthesis tool for the design of high-performance GBO. The tool is built on a GBO design methodology, which we proposed at the circuit part of this paper. We believe that, the proposed tool GBOPCAD can be included into an analog synthesis system for the design of high-performance opamps.

The remainder of the paper is organized as follows. The circuit fundamentals and the design methodology will be introduced in Section II. The implementation environment and the design context will be described in Section III. The development of GBOPCAD, accompanied by a sample TGBOP design will be covered in Sections IV and V. The GBOPCAD design results of the sample opamp will be shown in Section VI. Section VII gives concluding remarks.

## II. CIRCUIT FUNDAMENTALS AND DESIGN METHODOLOGY

### A. Gain Boosting Technique

The GBO employs two amplifiers: the main opamp and the gain boosting opamp (GBAmp). In Figs. 1 and 2, a telescopic GBO (TGBOP) and a folded-cascode GBO (FGBOP) are given, respectively. The dc gain of TGBOP can be expressed as

$$A_{dc} \approx \frac{1}{2} \frac{g_{m1}g_{m3}}{g_{ds1}g_{ds3}} A_{dcgb} \quad (1)$$

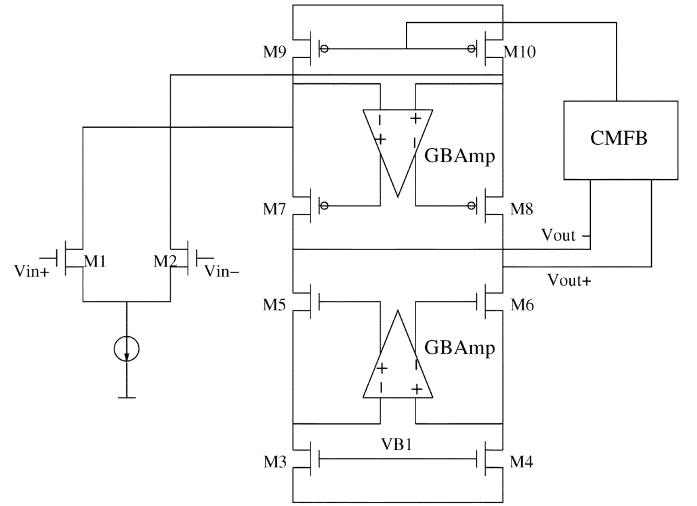


Fig. 2. FCGOP structure.

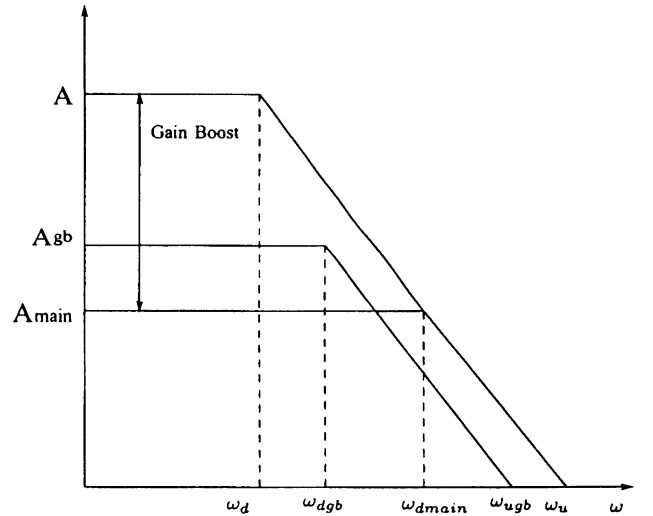


Fig. 3. Ideal gain-frequency chart of the GBO.

where  $A_{dcgb}$  is the dc gain of GBAmp. Hence, the ideal effect of the GBAmp is to improve the output impedance by  $A_{dcgb}$  times, which boosts the dc gain by the same amount.

The ideal gain-frequency chart of the GBO is shown in Fig. 3. At the low-frequency end, because the output impedance of the opamp is improved  $A_{dcgb}$  times by the GBAmp, the dominant pole at the opamps output node will be  $A_{dcgb}$  times lower in frequency

$$\omega_d = \frac{\omega_{dmain}}{A_{dcgb}} \quad (2)$$

where  $\omega_{dmain}$  is the dominant pole frequency of the main opamp. Also, the loads at the output node of GBAmplifiers are usually small, which will have the gain-frequency characteristic of GBAmplifiers to be a first-order rolloff. Ideally, on the dB-dB plot, the high-frequency performance of the GBO remains unchanged from that of the main opamp, except for a higher dc gain and a lower dominant pole as shown in Fig. 3. This characteristic enables GBOs to achieve high bandwidth and high gain at the same time.

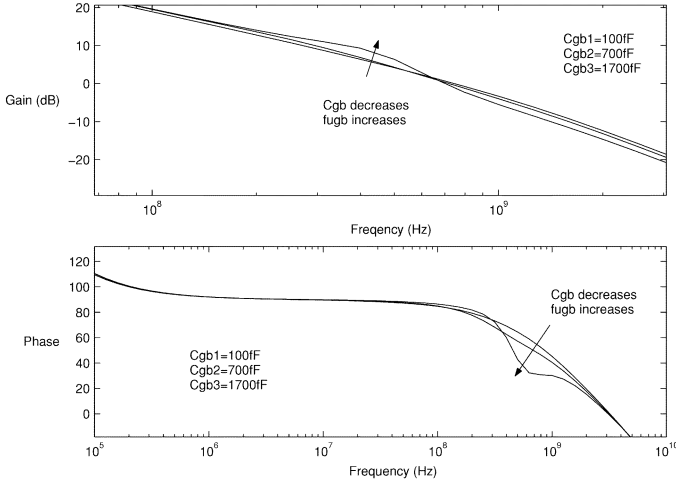


Fig. 4. ac performances with different GBamp compensations.

### B. Higher Order Effects

However, the characteristic of the GBamp has significant influence on the transient performance of the opamp. There are two potential problems that can affect the performance of the GBO.

As mentioned in [5], when the bandwidth of GBamp is not excessively high, there exists a doublet at the unity-gain frequency of the GBamp ( $\omega_{ugb}$ ). The doublet can be detrimental for the settling performance of the opamp, although it might not be easy to spot the existence of doublet on the opamps ac characteristic charts, as discussed in [7]. A common solution would be to push the doublet to a higher frequency.

However, at the high frequency, this effort can potentially lead to an instability problem. When the doublet is pushed near the nondominant pole of the main opamp ( $\omega_{ndmain}$ ), [8] and [9] reported the generation of a pair of complex conjugate poles. The attempt to push this pair of poles to higher frequencies would reduce the phase margin (PM) of the circuit.

To study these two effects, we plotted the ac and transient characteristics of GBO for different bandwidths of GBamps in Figs. 4 and 5. In Figs. 4 and 5, the same GBamp is subjected to different compensations, which changes the bandwidth of the GBamp accordingly. Using Matlab simulation, the major pole-zero evolution of GBO can be inferred, as shown in Fig. 6.

For large compensation, or when  $\omega_{ugb}$  is as low as at position A in Fig. 6, the doublet can be seen moving up in frequency as  $\omega_{ugb}$  increases. In this phase, the settling time reduces as  $\omega_{ugb}$  increases. When the doublet moves to a higher frequency, a pair of complex conjugate poles is generated, as reported in [8] and [9]. Further increasing  $\omega_{ugb}$  can push the complex conjugate pole pair up along the real axis, which continues reducing the opamps settling time. At the same time, however, it also pushes the poles away from the real axis, which gives way to oscillation in the time domain. Beyond some point, such as B, the pair starts to move back along the real axis while it continues moving away from the real axis. During this phase, the envelope settling time starts to increase instead, as does the oscillation frequency for the transient output. The dampened oscillation shows its way when the envelope settling time becomes longer than the oscillation period, such as at position C.

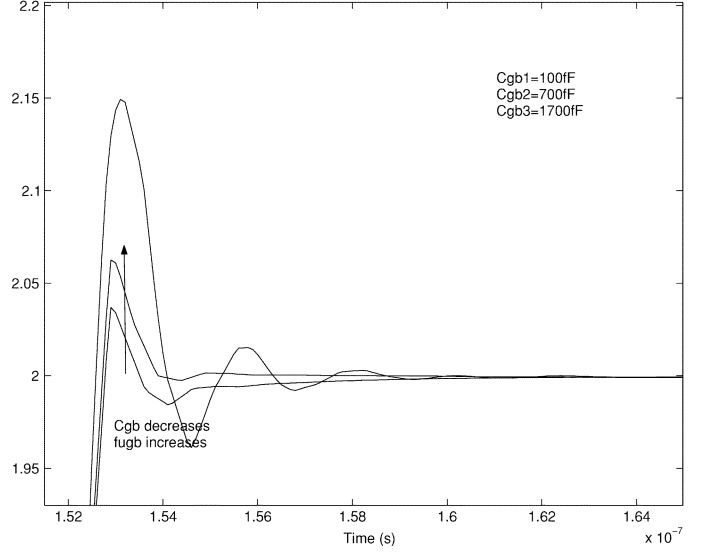
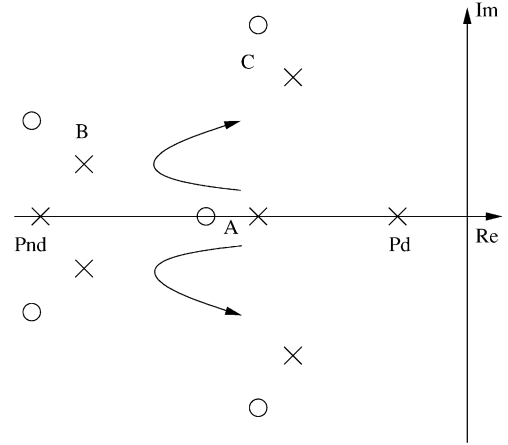


Fig. 5. Settling performances with different GBamp compensations.

Fig. 6. Pole-zero evolution of GBO with  $\omega_{ugb}$ .

Hence, there exists an optimal position in terms of the opamps settling performance. As a result, the design of the GBO need to include an optimization process to push up the doublet while keeping the system stable. A small compensation capacitance of several hundred femto-Farads is used for the GBamp to manage the optimization process.

### C. Design Methodology

Based on the studies in previous sections, a three-step design methodology can be followed for the design of GBOs.

Due to the decoupling of gain and bandwidth, the main opamp is designed during the first design phase. The objective in this design phase is to reach the constraints of bandwidth ( $f_u$ ), PM, voltage swing (VS), and the slew rate (SR).

During the second design phase, the two GBamps are designed. The objective in this design phase is to reach the gain ( $A_{dc}$ ) constraint, and to optimize the GBamp for highest non-dominant pole position ( $f_{ndgb}$ ), which is used potentially to achieve a high bandwidth for GBamp and to leave room for the settling performance optimization in the next phase.

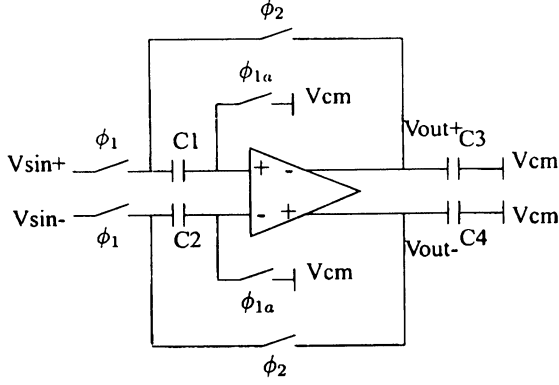


Fig. 7. S/H front-end.

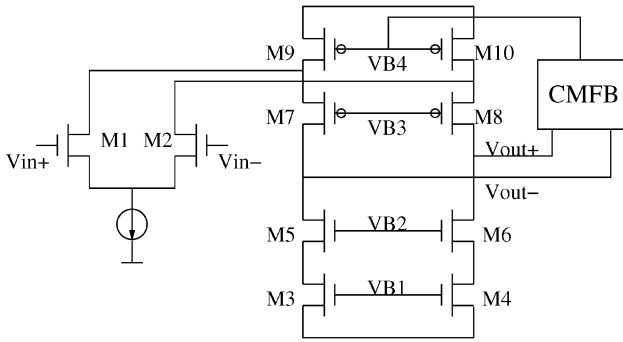


Fig. 8. GBamp circuit.

The last design phase is dedicated for opamp settling performance optimization. The objective in this design phase is to achieve the best settling performance ( $t_{set}$ ) of the GBO.

### III. IMPLEMENTATION ENVIRONMENT

The differential GBO is designed for a sample/hold (S/H) front-end of a 12-bit 50 Ms/s ADC, as shown in Fig. 7. Therefore, we will use Fig. 7 as a test bench for the final opamps transient performance testing. The circuit is designed in a 0.6- $\mu$ m CMOS process, with a supply voltage of 5 V. The differential signal swing range is  $-1.8 \text{ V} \pm 1.8 \text{ V}$ .

We choose the TGBOP topology of Fig. 1 for our design. However, the general rules of the methodology can readily be extended to the FGBOP shown in Fig. 2. In order to fulfill the dc level constraints, a folded-cascode structure is used for GBamps, as shown in Fig. 8. In order to reduce the capacitive load at the output, a continuous CMFB circuit, Fig. 9, is used in our design.

The synthesis tool, GBOPCAD, is written in Perl. Although the language is slow in speed compared to C, it gives us flexibility on inter-process operation under UNIX. Hence, it serves well as a prototyping tool. We use HSPICE as the evaluation tool for our design. GBOPCAD runs on a Sun Blade 1500 workstation, with a 1-GHz UltraSPARC IIIi processor and 2 GB memory.

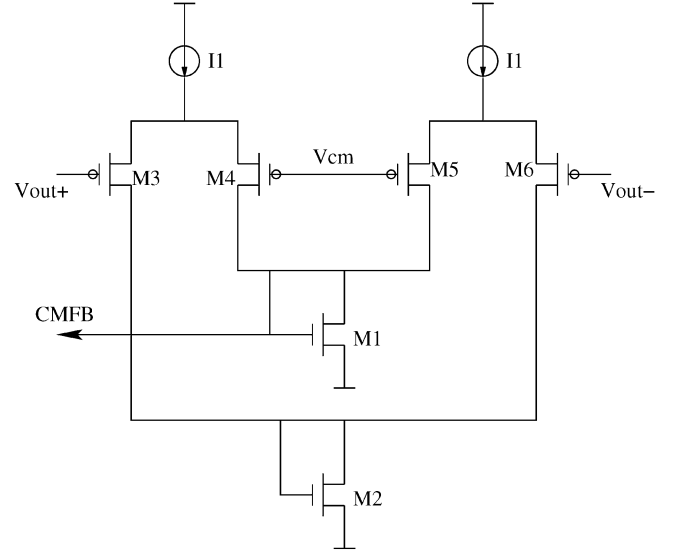


Fig. 9. Common-mode feedback circuit.

TABLE I  
SAMPLE SPECIFICATIONS FOR HIGH-PERFORMANCE GAIN-BOOSTED OPAMP

	Specification
Gain(dB)	> 80
Unity-gain bandwidth (MHz)	> 700
Phase Margin ( $^\circ$ )	> 60
Voltage Swing (V)	> 0.9
Slew Rate (V/ $\mu$ s)	> 800
Power Consumption (mW)	< 35

### IV. OVERVIEW OF GBOPCAD

#### A. Specification Conversion

Like most previously introduced CAD tools, such as GPCAD [11], OPASYN [14], DELIGHT.SPICE [15] and ASTRX/OBLX [16], GBOPCAD employs an optimization-based analog sizing approach for synthesis. Therefore, as a first step, the specifications of the synthesis problem should be transformed into the constraints for a constrained-optimization problem. Then, the constraints should be coded to formulate a cost function for the optimization problem.

In Table I, a sample of the specifications for high-performance GBO are listed. According to the applications, the specifications can be transformed into constraints in two categories.

1) *Strong Constraints*: These are the constraints that the design must meet. For example,  $PM > 60^\circ$  is usually a strong constraint, because below this margin, the circuit is prone to be unstable. During the optimization process, once a sizing configuration is found to fail any strong constraint, the configuration will be rejected immediately.

2) *Weak Constraints*: These are the constraints that the design should try to meet at its best effort. For example, for many applications, power consumption < 25 mW can be a weak constraint. The design goal of these applications is actually to obtain the minimal power consumption, on achieving the other specifications.

The classification of the two constraint types are important because different types of constraints will be codified differently

in the formulation of the cost function. However, the classification result is application specific. For certain applications, bandwidth can be of paramount importance. Then, the bandwidth specification will be a strong constraint, and the power specification can be a weak constraint, as in the example above. However, for other applications, to achieve a specified low power consumption might be important, then, the power specification becomes a strong constraint, while the bandwidth can become a weak constraint.

### B. Cost Function Formulation

The cost function of the constrained-optimization problem is generally formulated as (3). The objective of the problem is to maximize the cost function  $C(\vec{x})$  in the design space of  $\vec{x}$

$$C(\vec{x}) = \sum a_i S_i(\vec{x}) + \sum b_i W_i(\vec{x}). \quad (3)$$

Here,  $S_i(\vec{x})$  are the collective codified strong constraints, and  $W_i(\vec{x})$  are the collective codified weak constraints.

The codification of strong constraints is relatively easy, as shown in (4).

$$S_i(\vec{x}) = \begin{cases} -\infty, & \text{if strong constraint } i \text{ is not met} \\ 0, & \text{if strong constraint } i \text{ is met.} \end{cases} \quad (4)$$

However, the codification of weak constraints needs more discussion. Some previous work [16], [17] codified the weak constraints into exact equations. The advantage of this method is that the cost function can be measured in numerical values for any configuration. However, the problem is that circuit designers do not always feel comfortable at the idea of comparing bandwidth with power consumption, unless they are forced to. In other words, the exact way of codification can be contentious. Hence, in GBOPCAD, we resort to a different approach. We transform all the specifications into strong constraints, except one. With only one weak constraint, the cost function simplifies to (5)

$$C(\vec{x}) = \begin{cases} -\infty, & \text{if any strong constraint is not met} \\ W(\vec{x}), & \text{if all strong constraints are met.} \end{cases} \quad (5)$$

Here,  $W(\vec{x})$  is the direct variable in the weak constraint, such as bandwidth, or power consumption.

The only occasion that this cost function formulation method generates significantly different solutions than the previous method is when all the design specifications can not be met at the same time. At these moments, it would make more sense to have a circuit designer be actively engaged in changing to a new process, a new circuit topology, or recalculating the specifications, rather than leaving a programmed equation to make decisions.

### C. GBOPCAD Fundamentals

As described in Section I, equation-based tools can find an optimized solution in a short computation time, while their results are either inaccurate or not globally optimal. On the other hand, simulation-based tools can provide more accurate circuit results and have a better chance of finding the global optimum, at the cost of longer computation time, which can grow quickly

TABLE II  
SPECIFICATIONS FOR TARGET S/H FRONT-END

	Specification
Resolution	12 bits
Sampling Rate (MS/s)	50
Diff. Signal Range (V)	-1.8 ~ +1.8
Power Consumption (mW)	< 35
Capacitive Loads (pF)	2
Sampling Caps (pF)	4

with circuit complexity. The complementary nature of the two methods tantalizes us trying to combine the two methods. Although it is difficult to design a generic way to combine them, effective tools can be built specific to individual topology.

In GBOPCAD, SPICE is used to evaluate the performance of each sizing configuration to guarantee the accuracy. We also notice that analytic equations are valuable assets from previous experiences. Therefore, we use them as guidance for our adaptation process. Based on the equations and heuristics, we developed optimization algorithms, with groups of adaption rules, specific to the circuit under optimization. Because these algorithms are basically based on equations, which eliminates large number of impossible configurations from being evaluated, they can find a good solution in a short time, in the order of 10 minutes for our implementations. Although this solution is still crude, since all the space for possible “optimal” configuration has been sampled, there is a good chance that the global optimum locates close or has a close value to this good solution.

In the next step, GBOPCAD uses SA to search for the true global optimum. With a good starting point, SA has a better chance to find the global optimum in a short time.

## V. GBOPCAD DETAILS

GBOPCAD takes the opamp specifications as input, and generates an optimal sizing solution to meet the specifications. For our application, however, extra preparation need to be taken to convert the specifications for the S/H front-end in Fig. 7 to those for the opamp.

The specifications for S/H front-end are shown in Table II. From the resolution and sampling rate specifications in Table II, one finds that the opamp is required to settle to 0.0244% in 10 ns. If we make a conservative clock budget, the slewing process is allowed to last 5 ns, the overhead of clock skew is 2 ns and sampling clock is 1 ns ahead of the phase clocks, the opamp should linearly settle to 0.0244% in 2 ns. This results in a time constant of the opamp of 0.24 ns, according to (6), [19]. The unity-gain bandwidth of the opamp can easily be calculated, from (7), to be 663 MHz with the feedback factor  $\beta = 1$

$$V_{\text{out}}(t) = V_{\text{step}}(1 - e^{-t/\tau}) \quad (6)$$

$$\tau = \frac{1}{\beta\omega_u} = \frac{1}{2\pi\beta f_u}. \quad (7)$$

If the differential input signal sampled by C1–C2 is  $V_{\text{in}}$  during the sampling phase in Fig. 7, the output voltage is given by (8), during the hold phase. In order to achieve 12-bits accuracy of the output value, the error of the output voltage should be less

TABLE III  
OPTIMIZATION-ORIENTED CONSTRAINTS FOR MAIN OPAMP

	Constraint
Unity-gain bandwidth (MHz)	maximize
Phase Margin (°)	> 60
Voltage Swing (V)	> 0.9
Biasing Current (mA)	3.2 ~ 4.0

than half LSB. Therefore, the opamp is required to achieve a gain larger than  $20 \log(2 \times 2^{12}) = 78.3$  dB

$$V_{out} = \frac{1}{1 - \frac{1}{A_{dc}}} V_{in}. \quad (8)$$

Hence, the opamp specifications listed in Table I are indeed the target specifications for our design.

#### A. Main Opamp Design

1) *Optimization Problem Formulation:* As described in Section II, the objective in this design phase is to achieve the specifications of unity-gain frequency ( $f_u$ ), PM, VS, and SR of the main opamp. We also need to budget power consumption for each component in the GBO. The SR specification and the external load sets the lower bound of the biasing current for the main opamp in (9), which will be  $2 \times 800 \text{ V}/\mu\text{s} \times 2 \text{ pF} = 3.2 \text{ mA}$ . Therefore, we assign 20 mW to the differential stage of main opamp, 4 mW each to the differential stages of the two GBAs in Fig. 8. The remaining 20% of the power is to be assigned to the CMFB circuits in Fig. 9 and biasing circuitry. As a result, the optimization-oriented constraints for the main opamp are listed in Table III

$$SR = \frac{I}{2C_l}. \quad (9)$$

The biasing and CMFB circuitry are not performance determining components, although wrong configurations can lead to failure of the opamp. In GBOPCAD, they can be either chosen from the library or provided by users. The optimization is focused on the differential pair, as shown in Fig. 10.

The independent design variables in this optimization problem are  $W$ 's and  $L$ 's of MN1, MN3, MP1 and MP3, the gate voltages  $V_{out1}$ 's ( $V_{outn1}$ ,  $V_{outp1}$ ),  $V_{out2}$ 's ( $V_{outn2}$ ,  $V_{outp2}$ ) of the cascode transistors MP3 and MN3, and the biasing current  $I$ .

2) *Algorithm Description:* For the differential pair in Fig. 10, we have performance equations in (10) & (11). Based on the equations,  $g_m$  of MN1-MN2 need to be increased to optimize  $f_u$ . The nondominant pole  $f_{nd}$  of the differential pair need to be maximized, which requires minimal transistor sizes to reduce parasitics

$$\omega_u = \frac{g_m}{C_l} \quad (10)$$

$$\phi_{pm} = 90^\circ - \tan^{-1} \left( \frac{\omega_u}{\omega_{nd}} \right). \quad (11)$$

The major optimization procedure for the main opamp is shown in Fig. 11. It includes three major modules. The Bias Adapt module generates the minimal sizing configuration for the transistors to stay in the specified operation region under

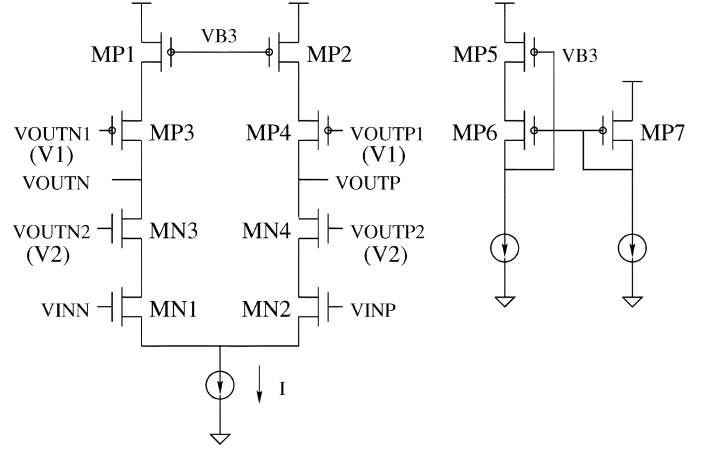


Fig. 10. Main opamp optimization problem.

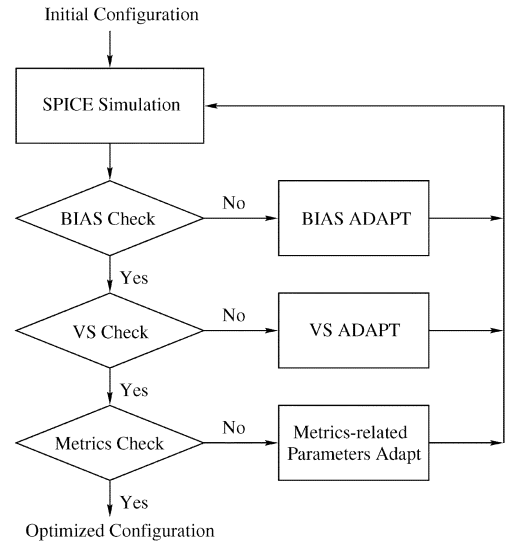


Fig. 11. Main optimizer for main opamp.

an external biasing condition. The voltage swing (VS) Adapt module is to optimize the sizing configuration for the VS specification. For the main opamp problem, the Metrics-related Parameters Adapt (MPA) module is to optimize the sizing configuration for PM and Bandwidth constraints. Inside of each functional module, a group of rules are designed based on the previous introduced equations and heuristics.

The optimizer in Fig. 11 optimizes the problem in the design space of transistors MN1, MN3, MP3 and  $V_{out1}$ ,  $V_{out2}$ , in an efficient way, which takes less than 1 minute for one run of the routine. At the outside of the optimizer, MP1 is sampled to find the best global solution, since there is no applicable heuristics available for the determining of MP1. The biasing current  $I$  steps up gradually in trying to minimize the power if possible. The complete procedure for main opamp design is given below.

#### Algorithm 1: Main Opamp Design

**INPUT:** PM constraint  $\Phi_m$ , VS constraint VS, minimal biasing current  $I_{min}$ , maximal biasing current  $I_{max}$ , allowed biasing range of each transistor BIAS, external bias voltage and load ENV;

TABLE IV  
OPTIMIZATION-ORIENTED CONSTRAINTS FOR GBamp1

	Constraint
Gain (dB)	> 45
$f_{ndgb}$ (MHz)	maximize
Biasing Current (mA)	< 0.8
Voltage Swing (V)	> 0.4
Output Voltage Tolerance (V)	< 0.1

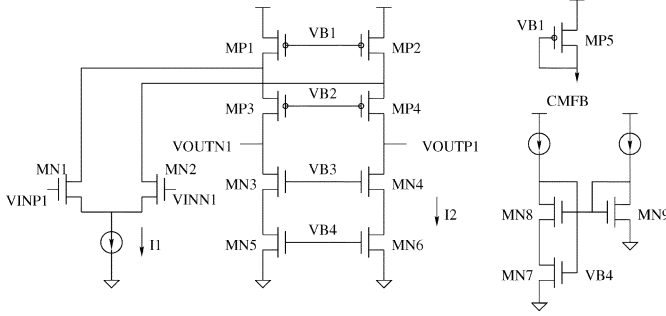


Fig. 12. Optimization problem of GBamp1.

**OUTPUT:** an optimized solution with W's and L's for every transistor, Vout1, Vout2 and I.

0.  $I := I_{\min}$ ;
1. **if**  $I > I_{\max}$ , **then** **Completes**;
2.  $(W, L)_{MP1} :=$  minimal allowed;
3.  $f_u := \text{optimizer}(I, (W, L)_{MP1}, \text{BIAS}, \text{ENV}, \Phi_m, \text{VS})$ ;
4. **if**  $f_u > f_{\max}$ , **then**  $f_{\max} := f_u$ ;
5.  $(W, L)_{MP1}$  increased;
6. **if**  $\text{CHECK}((W, L)_{MP1}) == \text{yes}$ , **then** **goto** 3;
7.  $I := I + \Delta I$ ; **goto** 1.

In the implementation of this routine, large granules are used in the adaption processes of MP1 and I to save computation time, because simulation annealing will follow this routine to fine the solution. At the meantime, because the MP1 and I space are globally sampled during this routine, the resulted solution should have a better chance to be close to the global optimum.

After running of this routine, several runs of plain SA with decreasing granule-size are followed. The annealing process stops when the resulted cost function stabilizes.

## B. GBamp Design

1) *Optimization Problem Formulation:* As described in Section II, the objective in this design phase is to achieve the gain specification ( $A_{dc}$ ) and maximize the nondominant pole position of GBamp ( $f_{ndgb}$ ). After the main opamp design, the gain of the main opamp ( $A_{dcmo}$ ) will be reduced from  $A_{dc}$  to obtain the gain constraint for GBamp ( $A_{dcgb}$ ). Because the dc output voltages of GBamps are actually Vout1 and Vout2 in the main opamp, they have to be kept close to the optimized value found in the previous design phase. A sample of the possible constraints for the optimization problem of GBamp1 is given in Table IV.

Again, the optimization focus is on the differential part in Fig. 12. The independent design variables in this optimization problem are W's and L's of MN1, MN3, MN5, MP1 and MN3,

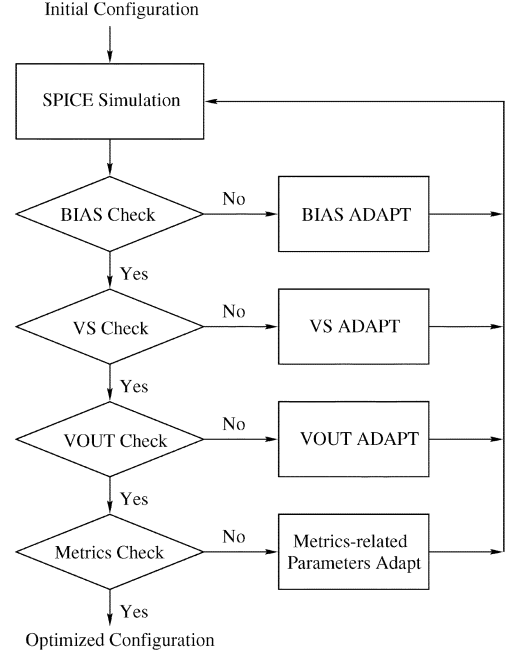


Fig. 13. Main optimizer for GBamps.

the gate voltages VB2, VB3 of the cascode transistors MP3 and MN3, and the biasing current I.

2) *Algorithm Description:* The gain of the opamp in Fig. 12 is given in (12). Thus, the gain can be adjusted either by increasing  $g_m$  of MN1-MN2 or by increasing the transistor sizes in the cascode stack to improve  $r_o$ . However, both efforts tend to lower the position of the nondominant pole. Therefore, the joint design space of the two efforts are sampled to find the optimal sizing

$$A_{dcgb} = \frac{1}{2} g_m r_o. \quad (12)$$

The major optimization procedure for GBamp is shown in Fig. 13, which is similar to that for the main opamp. The Bias Adapt and VS Adapt modules are responsible for similar functions as those in the main opamp optimizer. The VOUT Adapt module is used to tune the opamp into the allowed output voltage range. The Metrics-related Parameters Adapt module adapts the opamp for the gain and  $f_{ndgb}$  constraints. Again, groups of rules are designed based on equations and heuristics inside of each functional module.

The optimizer in Fig. 13 optimizes the problem in the design space of W's of MN1, MN3, MN5, MP1, MP3 and VB2, VB3, with a given  $r_o$  and bias current I1 and I2. Then, the L's of the cascoding stack are stepped through to provide the stack with different output resistance. Because the power consumption of GBamps is not critical for the total power of the GBO, the maximal biasing current will be chosen to provide the GBamps with best possible  $A_{dcgb}$  and  $f_{ndgb}$ . The complete routine for the design of GBAMP is given below.

## Algorithm 2: GBamp Design

**INPUT:** gain constraint  $A_{dcgb}$ , VS constraint VS, maximal biasing current  $I_{\max}$ , allowed biasing range of each transistor BIAS, external bias voltage and load ENV;

TABLE V  
MAIN OPAMP OPTIMIZATION RESULTS

	post-routine performance	post-SA per- formance
Gain(dB)	46.97	45.18
Unity-gain bandwidth (MHz)	816.9	888.94
Phase Margin (°)	60.0	60.0
Voltage Swing (V)	0.928	0.900
Biasing Current (mA)	3.6	3.6
Time (min.)	8	60

**OUTPUT:** an optimized solution with  $W$ 's and  $L$ 's for every transistor, V2B, V3B and  $I$ .

0.  $I := I_{\max}$ ;
2.  $L :=$  minimal allowed;
3.  $f_{\text{ndgb}} :=$  optimizer ( $I$ ,  $L$ , BIAS, ENV,  $A_{\text{dcgb}}$ , VS);
4. **if**  $f_{\text{ndgb}} > f_{\max}$ , **then**  $f_{\max} := f_{\text{ndgb}}$ ;
5.  $L$  increased;
6. **if** CHECK( $L$ ) == yes, **then goto** 3;
7. **Completes.**

Again, a sequence of plain SA with decreasing granule-size follows this routine to fine the optimal sizing solution.

### C. Settling Performance Optimization

The objective of the last design phase is to adjust the compensation of GBamps for the optimal transient response of the GBO. Therefore, GBOPCAD assembles the previously designed main opamp and GBamps into a GBO. The S/H front-end in Fig. 7 is used as the test-bench for this design phase.

## VI. OPTIMIZATION RESULTS

In this section, GBOPCAD is used to optimize for the opamp with the specifications given in previous sections.

First, the routine in Section V.A is followed to design the main opamp with constraints in shown Table III. In 8 minutes, a sizing solution is found, as listed in the middle column in Table V. Then, several runs of SAs are carried out. The annealing process completes after 4 rounds, when the annealed results of two successive runs varies less than 0.1%. The final optimized result for the main opamp is in the right column of Table V.

In this experiment, dozens more annealing runs are used to search for possibly a better "global optimum." However, no better solutions are found. Therefore, the final solution in Table V has a good probability to be the global optimal sizing configuration for the constraints in Table III. As we can see, the proposed main opamp design routine is able to generate a solution close to the global optimum within a short computation time.

Next, the GBamp design routine is followed to compute the optimal transistor sizes for GBamp1, with optimization constraints generated in the way introduced in Section V.B. The optimized results after the design routine are listed in the middle column of Table VI. The results of the found global optimum after SA are shown in the right column of Table VI. The design

TABLE VI  
GBAMP1 OPTIMIZATION RESULTS

	post-routine performance	post-SA per- formance
Gain(dB)	36.49	37.19
$f_{nd}$ (GHz)	1.259	1.349
Vout (V)	3.063	3.074
Biasing Current (mA)	0.8	0.8
Time (min.)	2	28

TABLE VII  
GBAMP2 OPTIMIZATION RESULTS

	post-routine performance	post-SA per- formance
Gain(dB)	34.98	39.44
$f_{nd}$ (GHz)	1.778	2.138
Vout (V)	2.898	2.998
Biasing Current (mA)	0.8	0.8
Time (min.)	4	28

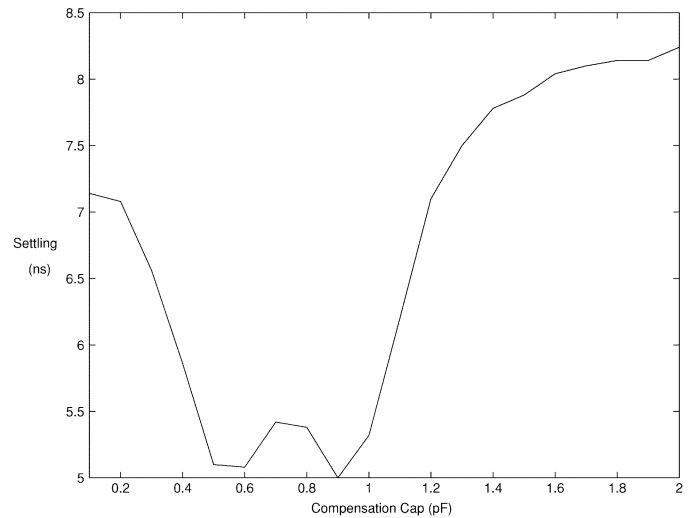


Fig. 14. Settling time changes as a function of compensation capacitance (or bandwidth) of GBamp.

results for GBamp2, after the GBamp design routine and SAs, are shown in Table VII.

Next, the GBO is assembled with the designed main opamp and GBamps. The S/H front-end in Fig. 7 is subjected to a differential rectangular input signal with amplitude of  $\pm 1.8$  V to test the opamps transient performance under worst slewing condition. GBOPCAD adjusts the compensation capacitors of GBamps to find the optimal settling position. A measurement of the relationship between the compensation capacitors of GBamp and the 0.0244% settling time of the opamp is shown in Fig. 14. Because the slewing time is difficult to identify during the measurement, the settling time in Fig. 14 is actually the result of both slewing and linear settling. A window of relatively low settling time exists as seen from the measurements. Outside this fast-settling window, the settling process is found to be rather slow. This justifies the inclusion of the final transient performance optimization phase by the GBOPCAD.



TABLE VIII  
CHARACTERISTICS OF FINAL DESIGNED GAIN-BOOSTED OPAMP

	Performances
Gain(dB)	80.77
Unity-gain bandwidth (MHz)	835.9
Phase Margin ( $^{\circ}$ )	60.15
Voltage Swing (V)	0.9
Settling time (ns)	5.0
Power (mW)	33

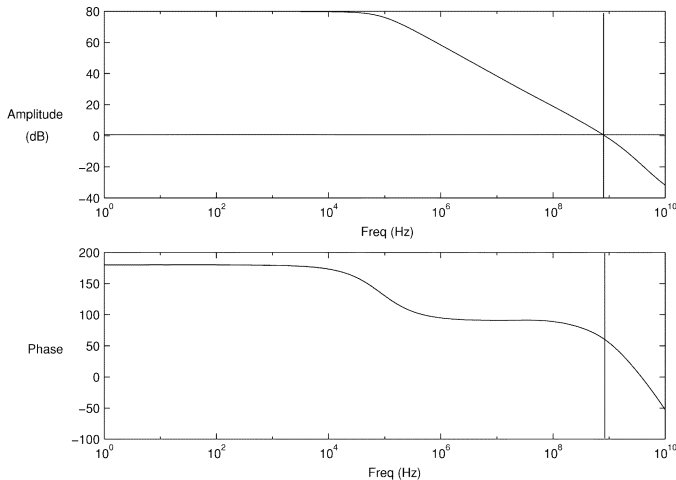


Fig. 15. Frequency characteristics of the final designed GBO.

The fundamentals of this behavior has been discussed in Section II. Also, the window has a fair size and a relatively flat floor. This enables the designs from GBOPCAD to be robust against temperature and process variations for applications. For our optimized opamp, the optimal 0.0244% settling time is 5 ns, including slewing and linear settling.

By now, a GBO design has been completed by GBOPCAD. The final optimized opamp achieves the characteristics in Table VIII. The frequency response of the opamp is shown in Fig. 15. The designed opamp is able to meet the specifications for a S/H front-end of a 12-bit 50 MS/s pipeline ADC. In order to test the linearity of the designed opamp for the S/H front-end, a 512-point FFT test is carried out for the front-end, with the result shown in Fig. 16. The differential input sinusoidal signal has a frequency of 8.1 MHz, and an amplitude of 1.8 V. The overall SNR is 81.9 dB, which is good enough for 12 bits resolution.

The whole process of finding the global optimum lasts about 2.5 h using a 1-GHz UltraSPARC IIIi processor and 2 GB memory, with time usage of each component listed in related tables. However, for each component, the design procedures that we proposed in Section V are shown to be able to generate sizing solutions that are close to global optima. Therefore, the majority time spent for simulated annealings to find global optima might not be justified for many applications that have less stringent specifications. For those applications, the design process can be accomplished in 0.5 h by running GBOPCAD without SAs.

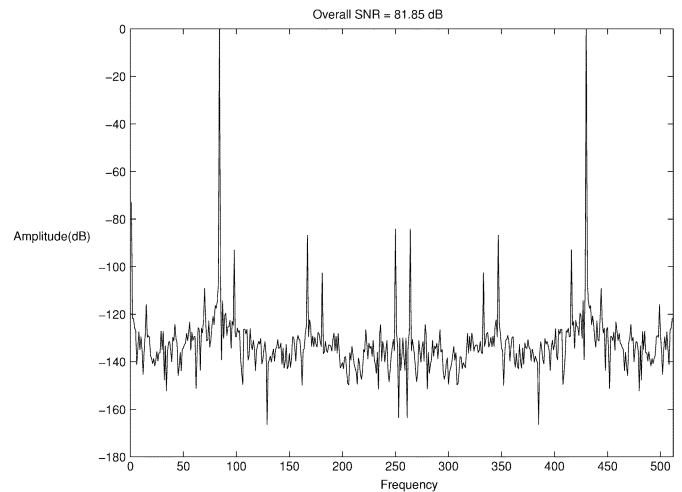


Fig. 16. 512-point FFT result for the designed S/H front-end.

## VII. CONCLUSION

High-performance opamps are essential for the design of high-speed high-resolution pipeline ADCs. In this paper, the properties of GBOs are studied. Based on the study, a new methodology is proposed for the design of high-performance opamps.

An automatic tool GBOPCAD is developed to design GBOs following the proposed methodology. In order to improve the accuracy of the design, GBOPCAD uses SPICE as the evaluation tool. In order to increase the probability of finding the global optimum, and to reduce the time of reaching it, GBOPCAD first generates a good design close to the global optimum by establishing groups of rules based on equations and heuristics. Then, GBOPCAD employs SAs to search for the global optimum from the “good” initial configuration. As a result, GBOPCAD is able to provide an accurate global optimal design in relatively short time. For applications with loose specifications, GBOPCAD is able to generate a good design close to global optimal within short time that is comparable to the one used by equation-based CAD tools.

Using GBOPCAD, a gain-boosed opamp with high-gain, high-bandwidth and short settling time is designed for our application of a 12-bit 50 MS/s pipeline ADC.

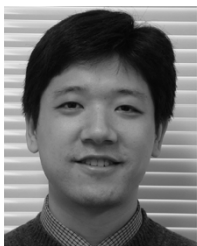
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